NEXT GENERATION X-RAY MONITOR FOR BUNCH-BY-BUNCH MONITORING OF NANOMETER BEAM SIZES AT THE WORLD'S HIGHEST LUMINOSITY PARTICLE COLLIDER

A THESIS SUBMITTED TO THE GRADUATE DIVISION OF THE UNIVERSITY OF HAWAIʻI AT MĀNOA IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF SCIENCE

IN

ELECTRICAL ENGINEERING

DECEMBER 2018

By

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ACKNOWLEDGMENTS

I would like to acknowledge the University of Hawaii at Manoa (UH Manoa) - Instrumentation Development Laboratory (IDLAB) for supporting this work. I would also like to thank my research advisor, Prof. Gary Varner, for giving me the opportunity to work and grow as an engineer in the lab. Many thanks to Matt Andrew for designing the laser test bench and mechanical structure of XRM. I could not have done this project without your advice. I would also like to thank Martin Bessner, Shawn Dubey, and Gang Liu for all of their feedback. I would also like to thank my family for supporting me through this hardship. I would like to further thank everyone at IDLAB for their support.

Finally, I would like to thank all of the committee members, Prof. David Garmire and Prof. Victor Lubecke, for their time and advice

ABSTRACT

Synchrotron radiation is commonly used in accelerators to monitor particle orbits. In most cases, these monitors are slow to read out and the digitizer's data typically do not include the information on individual particle bunches. After the announcement to upgrade KEKB to Super-KEKB, it was recognized that with a vertical beam-size of nanometers, to improve luminosity at the interaction point, there is a need for faster sampling and an ultra-low noise detector to monitor the beam and to determine beam-beam effects. The construction of the bunch-by-bunch X-ray Monitor (XRM) began in 2011, along with a new detector called Belle II. The University of Hawaii at Manoa was tasked with three detectors (KLM, iTOP, and XRM). An improved version with new XRM sensors, amplifier design and an improved electronics aims to address the weaknesses uncovered in previous XRM versions. This thesis covers the design details of the next generation of x-ray monitors, analysis from preliminary data collection at the local test stand, and the preparation done for testing at the KEK photon factory.

CONTENTS

CHAPTER 1
INTRODUCTION/BACKGROUND

1.1 Super KEKB/ Belle II Project.

Kō Enerugī Kasokuki Kenkyū Kikō Institute "KEK" (English : High Energy Accelerator Research Organization), based in Tsukuba, Iberkaki, Japan, is currently developing a new e^+e^- collider, called Super-KEKB. This is a major upgrade to the pre-existing e^+e^- KEKB collider. Its final target is 40 times higher luminosity than that of its predecessor in order to study flavor physics at its experiment, Belle II [15]. Unlike the symmetric energy collisions at CERN's Large Hadron Collider (LHC), Super-KEKB uses asymmetric collision energies to give produced particles a boost in the laboratory frame. These two rings are named Low Energy Ring (LER) and High Energy Ring (HER) and have an energy level of 4 GeV and 7 GeV, respectively. Positrons will be accelerated by the LER and the electrons are accelerated by the HER. The project is subdivided into three phases, with each phase incrementally increasing the beam current until the penultiumate beam current is reached during phase 3. Phase 2 recently ended and first collisions were achieved with an average vertical beam-size of $3\mu m$, at a bunch spacing of 6ns [15]. At Super-KEKB, the design goal is a vertical beam size at the interaction point of approximately 50 nm with bunch spacing of $\approx$ 2ns.

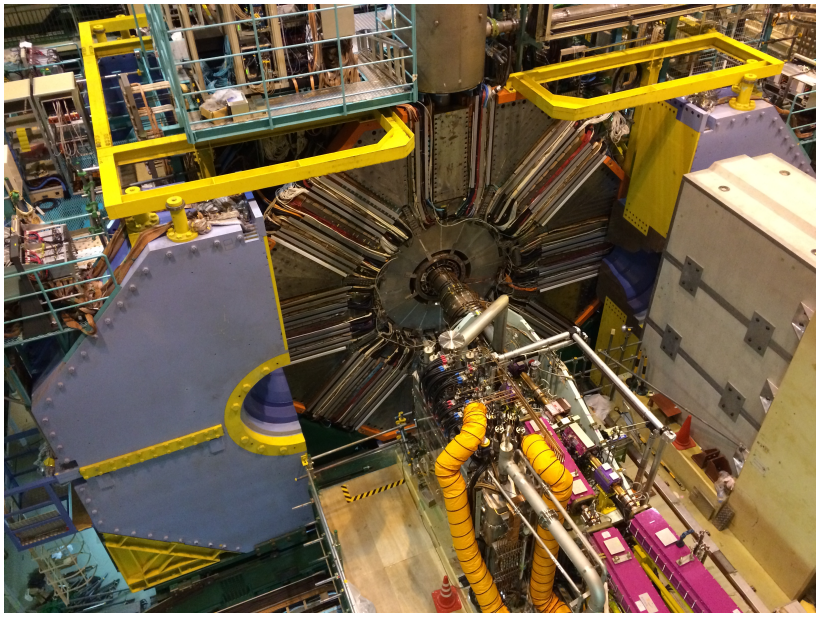


Figure 1.1: An image of the Belle II Detector at Super-KEKB, located at the interaction point of the accelerator. University of Hawaii Manoa was involved with two of the Belle II's subdetectors: iTOP and KLM. The image was taken by Dr. Martin Bessner

At the end of Phase 2, the vertical beam size was approximately 330μm at the interaction point. Figure 1.2 shows the time table for the progress of the average vertical beam size at the interaction point.

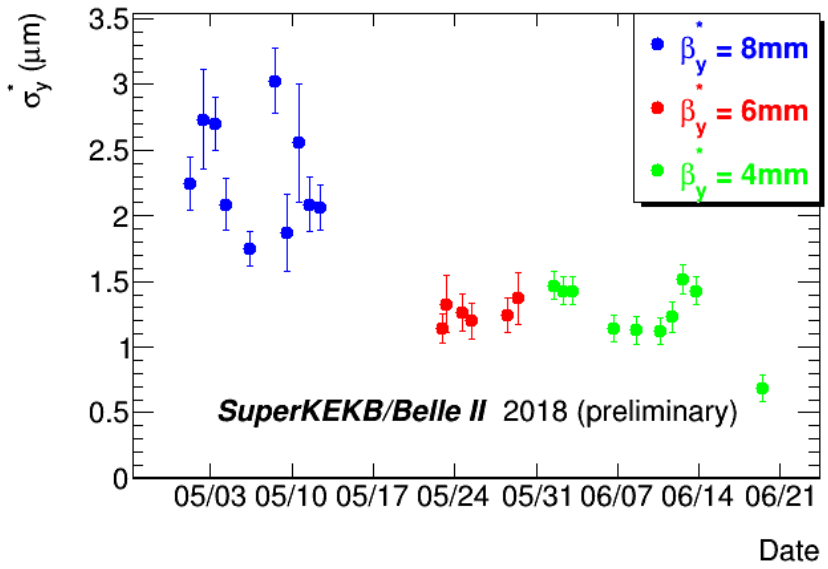


Figure 1.2: An Image of beam-crossing progress at Super-KEKB. The cross-section is progressing toward the intended final target of 50nm

The increase in luminosity of Super-KEKB with respect to KEKB is mostly due to a much stronger focusing of the colliding beams, leading to a decrease in the vertical beam bunch size at the interaction point (σ_y). The increase in bunch current is only increased by a factor of around two. Figure 1.3 shows schematic images of crossing beam bunches in KEKB and Super-KEKB, clearly showing the tighter focusing of the Super-KEKB beams.

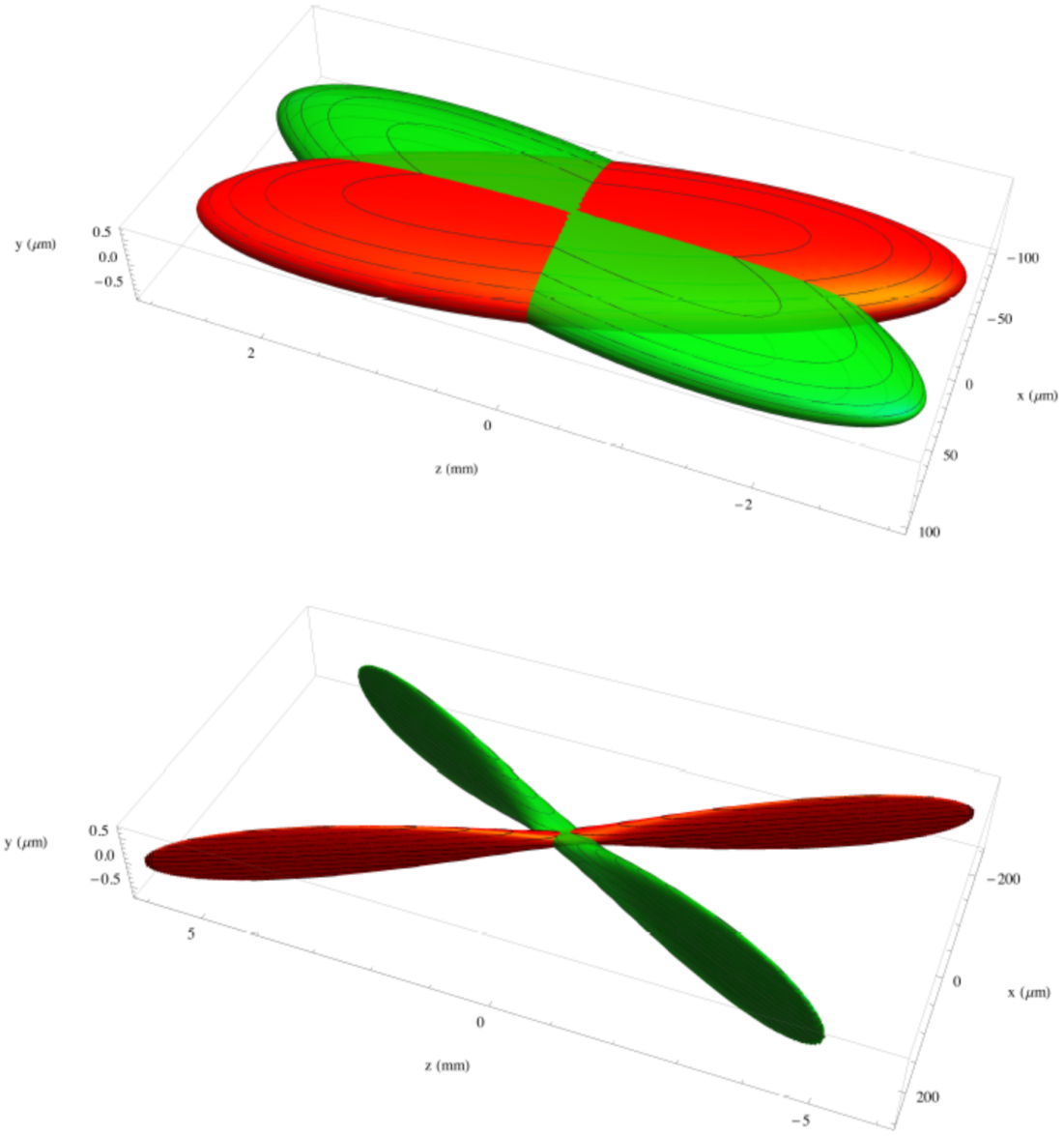


Figure 1.3: The bunch crossing schemes of KEKB and Super-KEKB. [15]

Table 1.1: Machine parameters for the KEKB and SuperKEKB [6, 8–11].

Parameter		**KEKB** Achieved LER/HER	**SuperKEKB** Nano-beam scheme LER/HER	**Unit**
Beam Energy	E_b	3.5/8.0	4.000 / 7.007	GeV
Beam current	I	1.64/1.19	3.6/ 2.6	A
number of bunches/ring	n_b	1585	2,500	
Circumference	C	3,016	3,016	m
Half Crossing angle	ϕ_x	11	41.5	mrad
Horizontal Emittance	ε_x	18	3.2/4.6	nm
Vertical Emittance	ε_y	360	8.64/11.5	pm
Horizontal β function	β_x^*	1200/1200	32 /25	mm
Vertical β function	β_y^*	5.9/5.9	0.27/ 0.41	mm
Horizontal beam size	σ_x^*	147/170	10.2 /7.75	µm
Vertical beam size	σ_y^*	940	59	nm
Bunch length	σ_z	$6 \sim 7$	6/5	mm
Beam-beam parameter	ξ_y	0.129/0.09	0.09/0.0875	
Luminosity	$\mathcal{L}$	2.11	80	$\times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$

The LER (Low Energy Ring) is the positron ring and the HER (High Energy Ring)is the electron ring. The * indicates values at interaction point (IP).

Table 1.1: The table of specifications for the KEKB and Super-KEKB.[14]

Large datasets for physics will be taken in Phase 3, expected to start a in early 2019. The beam monitor needs to be installed before the first physics run starts to give better understanding of the individual bunch sizes before passing through the interaction point. All seven Belle sub-detectors as well as the DAQ and trigger subsystems were upgraded during the time of transition from Belle to Belle II (simultaneous with the transition from KEKB to Super-KEKB). Two of the Belle II subdetectors' electronics (iTOP and KLM) were developed and tested at the University of Hawaii Manoa IDLAB. The XRM is UH's contribution to Super-KEKB and construction of the new version of the XRM will be the main focus of this thesis.

1.2 Synchrotron Radiation

Synchrotron radiation is electromagnetic energy emission from accelerated charged particles (such as electrons or ions) experiencing a magnetic field, resulting in a curved trajectory. For fast particles ($v \sim c$) the emission is mainly along a tangent to the particle path. The angular distribution of the emitted synchrotron radiation is related to the size of the radiating bunches. The XRM system is designed to measure the beam size with bunch-by-bunch resolution to determine possible beam-beam effects on the bunch size while in orbit. The total radiated power by a charged particle can be calculated with the equation

$$P_{total} = \frac{e^2 c}{6\pi\epsilon_0 (m_0 c^2)^4} \frac{E^4}{\rho^2}$$

The radiated power from a solid angle

$$\frac{dE}{d\Omega} = \frac{1}{c^3 \mu_0} \frac{\epsilon^4}{4\pi\epsilon} \frac{\beta^4}{\rho^4} \frac{(\beta^2 - 1) sin^2\Theta cos^2\phi + (1 - \beta cos\Theta)^2}{(1 - \beta cos\Theta)^5}$$

Using the general equation form of the beam's energy per solid-angle, the expected beams from the positron and electron are shown plotted below.

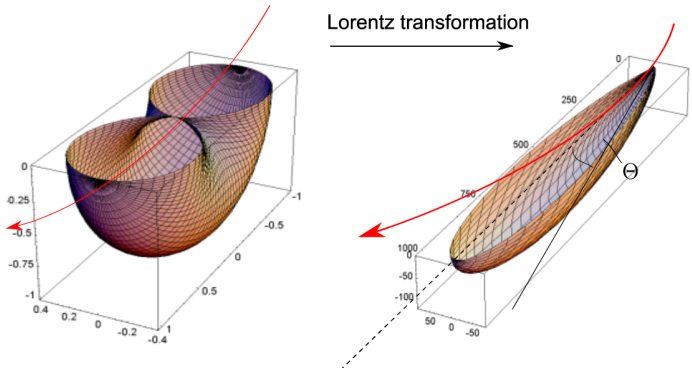


Figure 1.4: The beam profile when relativistic effects are considered

For SuperKEKB, the source of the magnetic field is placed approximately 43m from the detector box.

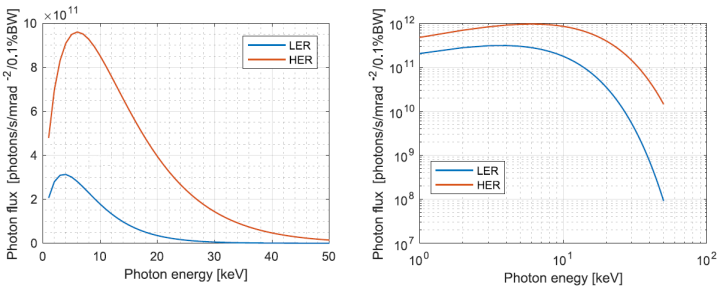
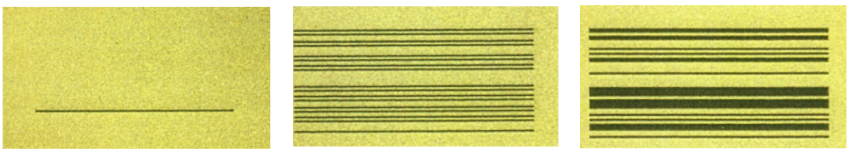


Figure 1.5: The beam profile with consideration of relativistic effects.

The XRM sensors were designed to be sensitive in the x-ray band; the x-ray band and the visual spectrum band are measured using different detectors.

1.3 Coded Aperture Filter

In order to project the synchrotron radiation onto the XRM sensor, in principle a single slit "pin-hole" aperture filter would be sufficient. The size of the beam bunch could then be obtained by measuring the width of the distribution of detected X-Ray photons as shown in Figure 1.7a. However, the photon yield of a single slit aperture is too low. Increasing the number and width of slits in the aperture filter increases the overall yield of photons on the sensor, but generates more complex patterns on the sensor plane, as is shown in Figure 1.7b/c. Initially phase 1 was tested with a single pin hole sized filter. The coded aperture in combination with a the pin hole masked aperture is used for phases 2 and 3. There are two types of apertures, one each for the LER and HER. These apertures are specially made for the XRM and are 800μm thick diamond substrates with 20μm thick gold patterns. The substrate was chosen due to the filters being subjected to the synchrotron beam path. [14]



(a) Pinhole **(b)** Multi-slits **(c)** URA

Figure 1.6: Mask pattern (pinhole, 17 multi-slits, and 12-slits URA) for both rings.[14]

The final aperture expected has 12 slits and the images showing the number of photons/pixel for single-pass 1 mA bunches, for different beam sizes in the LER, are shown, in Figure 1.7.

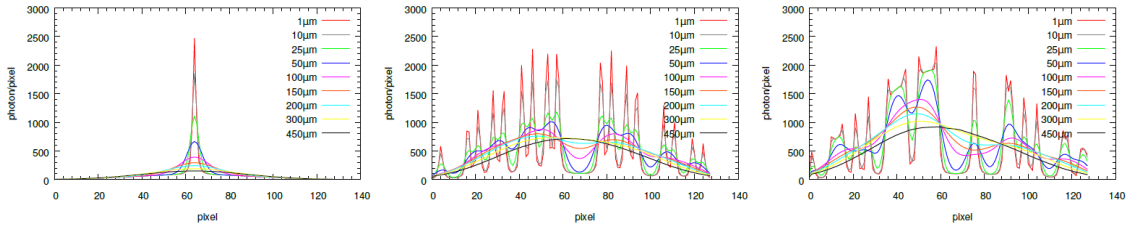


Figure 1.7: Simulated detector images showing the number of photons/pixel for single-pass 1 mA bunches, for different beam sizes in the LER. A series of detector image templates are generated for a range of beam sizes, and these are then compared with the data to find the closest match. (a) Pinhole mask, (b) multi-slits mask consisting of 17 peaks, and (c) URA mask consisting of 12 peaks. The number of peaks represents the number of slits that allow light to pass through[14]

The simulation is still in its preliminary stage. The result does not take into account the increasing beam current during phase 3.

1.4 Detector Box

Two custom designed metal boxes with beryllium windows along the beam path were built for this application. The detector, inside of the metal enclosure, is mounted to an X-Y translational stage and rotation arms for sensor-to-beam alignment. They are mounted to a solid aluminum optical bullet board base. The box is currently located at KEK and it was built to prevent the X-ray portion of the synchrotron beam from ionizing the atmosphere, generating unwanted nitrogen florescence and ozone molecules. The box is designed to be pressurized during the final installation of the detector. The pressurized box will be filled with helium to replace the atmosphere.

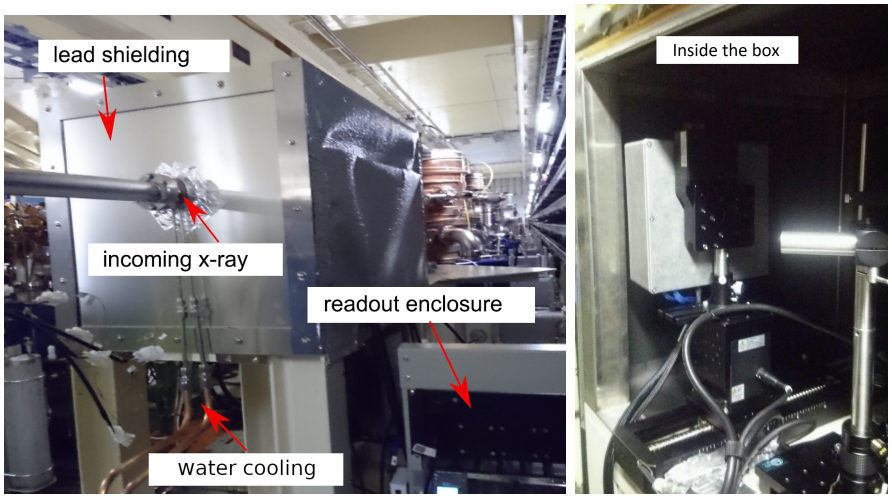


Figure 1.8: The detector box built at Fuji Hall, KEK.[14]

Two x-ray monitoring systems are needed to monitor the vertical beam-size for both the LER

and HER. Two monitors will be placed opposite the ring, thus two similar boxes were built at KEK; one at the Oho Hall, for monitoring HER and one at Fuji Hall side for monitoring LER.

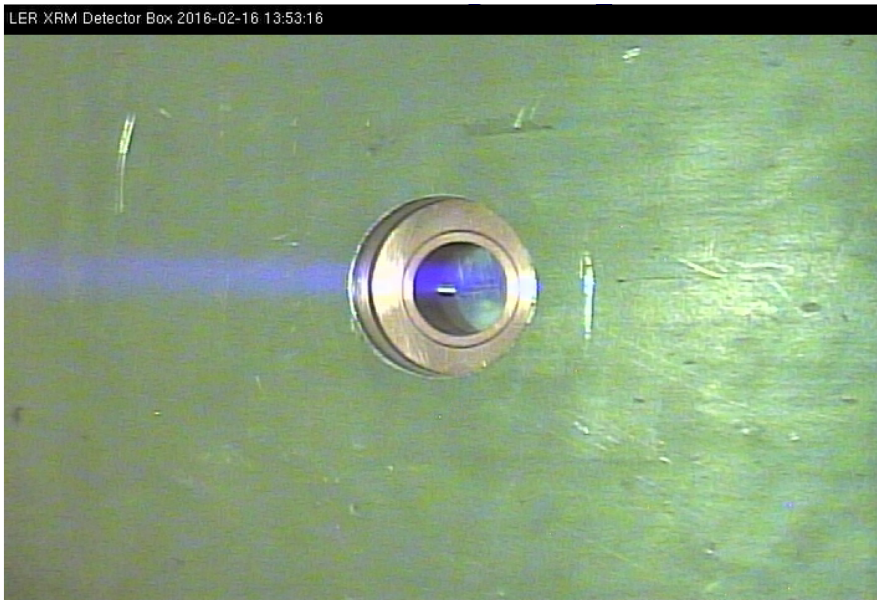


Figure 1.9: The image at the window of the detector box during the phase 1's beam test. The purple glow seen near the windows is the nitrogen fluorescence due to the beam interaction with the atmosphere. As a consequence of beam interactions with atmosphere, ozone is generated by the surrounding air, and is a source of danger. The beryllium window was chosen for its optical properties.

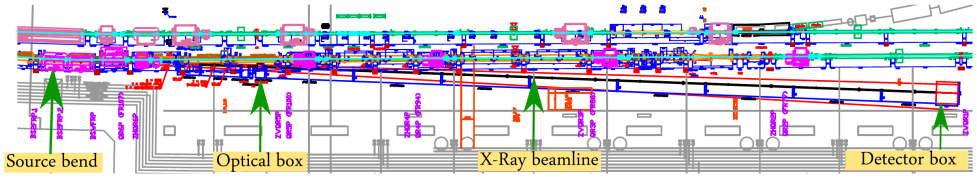


Figure 1.10: The installation of the box location relative to the bending magnet at Fuji Hall side. [14]

For testing done at the photon factory, the sensors need a detector box. The beam intensity at the photon factory is expected to be considerably less than the final intensity. During testing of the detector at the photon factory, the detector will be mounted on a stationary mount. The final placement of the detector will be mounted on a rotational arm with fixed structures that is designed for ease of detachment of the electronics portion from mechanical portion of the detector. The details of the current detector design are discussed in chapter 2

1.5 In-house Testing Structure

For the primary testing done at the University of Hawaii Manoa, there is not an x-ray source readily available, thus, an IR laser is be used as a substitute for the photon source. The electronics are placed into electromagnetic interference (EMI) shielding, since the high current pulse needed to drive the laser pulse couples to the sensor. A shielded box will only be used to test the basic functionality of the sensors as the front-end is developed. The sensor is exposed to a 980nm laser diode emission, and coupled through the box by fiber optics and placed inside the EMI box.

A fanout board is mounted to the sensor board that breakout four out of 128 anode pins to an SMA cable, for the evaluation of amplifier designs.

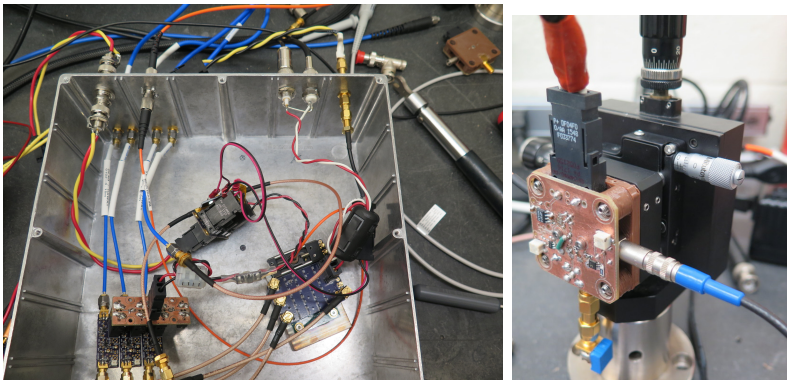


Figure 1.11: The EMI shielded box used during the initial testing phase of the sensors. All electronics are present inside the box except for the laser diode [14]

The sensors/front-end electronics read out details are further elaborated on in the read out detector section of this thesis. The primary purpose of these stations was to test the functionality, characteristics and stability of the overall system.

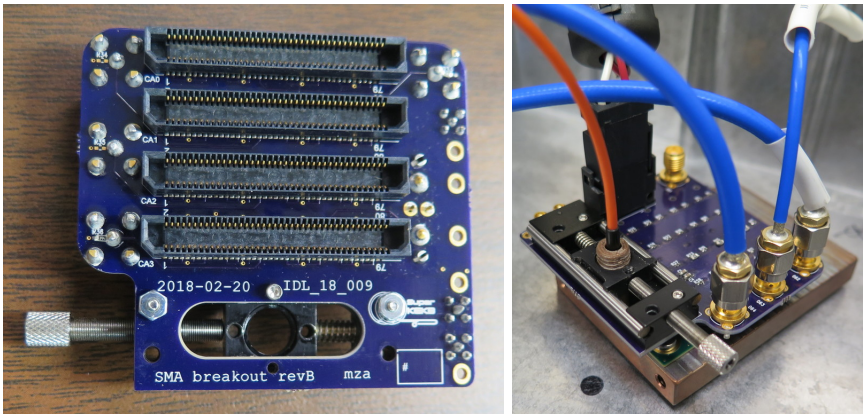


Figure 1.12: The breakout board for the ERM8 to SMA connector. The board was designed by Matt Andrew[14]. It was built for bench-top testing purposes and it allows sensors to be connected to various amplifiers to determine the stability of the system.

The initial testing phase using the testing station was done to validate the functionality of the new sensor and determine the sensor's characteristics. After that, the sensor's outputs were connected to a different amplifier and was tested using this test station, and evaluated using a oscilloscope and laser source.

1.6 Previous Revision

This section will briefly discuss the the previous detector and some of the lessons learned from the previous generation. Since the author was not involved in the development cycle at the time, the topic is a brief description of the functionality and the advice for the next iteration. The next chapter will go into the current revision of the detector design.

1.6.1 Pre-amplifier/Sensor Boards

The RF amplifier used for amplification was a PSA-545+ from Mini-Circuits. The preamplifiers were combined with the sensor board to reduce transmission line length and other parasitic noise factors.

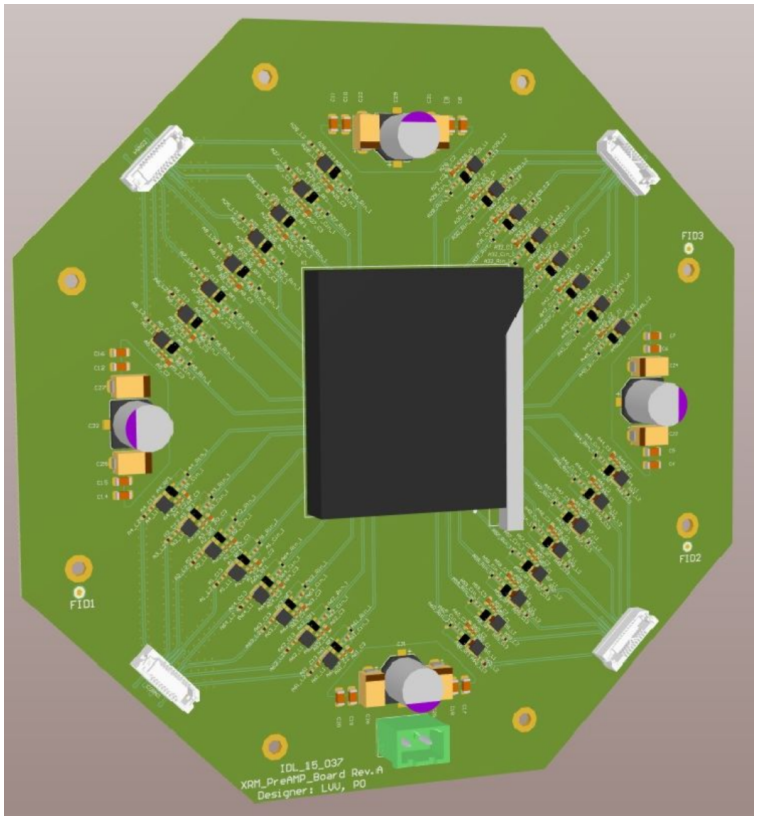


Figure 1.13: The image shows the previous generation preamplifier. The board was designed by Vihtori Virta. The sensor on this board was a commercial product to reduce the development time.

It was powered by a single 5V rail and the sensor's bias was on board. The inputs were AC coupled and terminated to 50 Ω, the output of the amplifier went to another variable gain amplifier board connected through a SAMTEC Edge-rate 40pin connector.

Unlike the previous revision, where no pulse was seen, this revision shows actual pulses from the sensors that showed a potential to be a working design. However, there were still issues that needed to be addressed with next revision. The AC coupling on the input stage caused it not to return to baseline fast enough thus making the raw signal pedestal subtraction difficult and in turn, making the preamplifier useless for a high event rate source, such as the bunch-by-bunch monitoring of this accelerator. The source of the baseline was not determined since the initial test with the laser pulse of the previous revision showed no instability on the signal. It was suggested that having a DC coupled amplifier may be better at returning to baseline since we can actively control the detector strip voltage. For this iteration, the goal of the design is to not use a RF amplifier since most of these type of amplifiers required AC coupling for their functionality. The purpose of this thesis will cover the commercially available DC capable amplifiers and whether they can meet the design criteria. The details of the amplifier choice will be discussed in detail in "CHAPTER 3 : Amplifier Chains"

1.6.2 Variable Gain Amplifier Stage Board

The variable gain amplifier board was designed to be able to change the gain from 6dB to 60dB. The design used the same amplifier used in the preamplifier (PSA-545+) RF amplifier chains. It is used to set the preferred gain of the overall system before the digitizer board. The board's outputs are custom connectors that were designed to be mountable on the iTOP module's pogo pins.

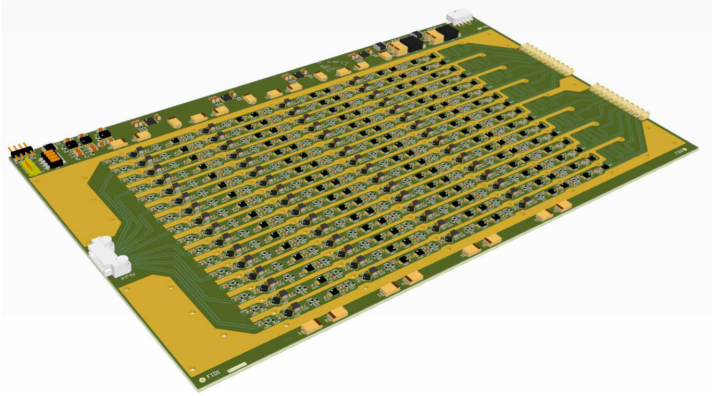


Figure 1.14: The image shows previous generation variable amplifier. It was designed by Peter Orel and it was designed to be as flexible in terms of amplification as possible, due to the lack of SNR information of the sensors and its signal output.

However there were several drawbacks with the design which was desirable, first the pogo pins

were hard to fully seat properly, making it difficult determine whether the pogo pins connection on the iTOP module were fully engaged. Only a single channel of the board was fully populated for testing purposes, thus, it is not determined if this is a real issue in the fully populated board design. Another issue is the necessity of the secondary amplifier chains physical aspects as it was too bulky to be mounted to the rotational arm and required custom coaxial connections between the preamplifier to the input of the variable amplifier.

After performing the laser test on the test stand, the data showed that the variable gains were not necessary since the sensor's signal was fully saturating the IRSX dynamic range from the preamplifier stage alone. The final tests showed that the sensors required only 20 dB of gain per channel. The previous revision used different sensors from this revision (Fermionics sensors), as such, the final design may need more gain. For this iteration, the current design strategy is to remove the usage of a variable gain stage and opt to use only two stage amplification to allow a flexible range but require a minimum gain of 20dB.

CHAPTER 2
DETECTORS

This chapter will discuss the photo-element and the electronics that complete the detector. This section will provide general information about scope and specifications. The electronics section will follow the optical signal from the photo-sensors to readout electronics where the dataset is aggregated at the detector. After that, we will discuss the mechanical structure and previously done thermal simulation that influenced the current mechanical design.

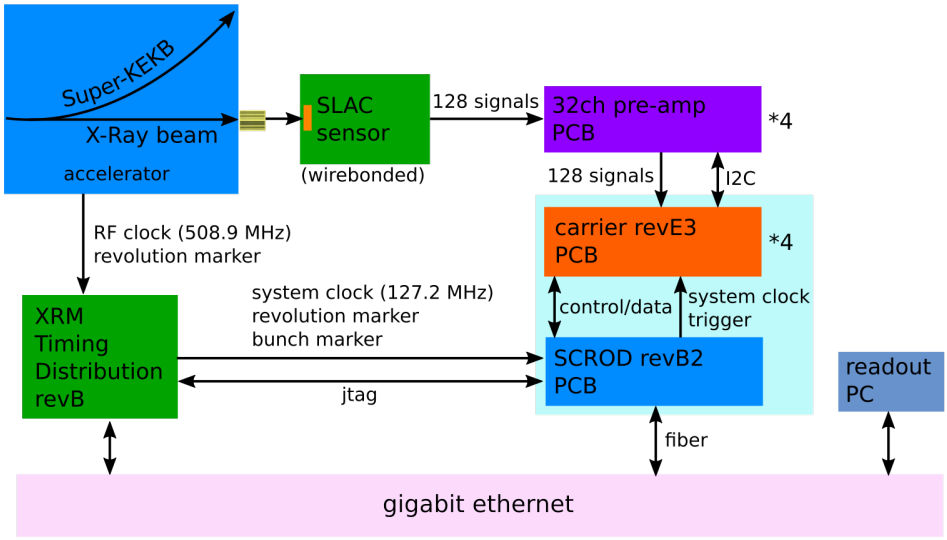


Figure 2.1: Shows the general overview diagram of the detector.

After brief coverage each of the detector's sections, the author's contributions for the latest revision of XRM will be discussed.

2.1 SLAC Strip Sensors

2.1.1 Photo-diode Operation

The photo-diode is a P - N junction diode. It uses the production of electron-hole pairs to generate a photo-current when exposed to a photon. The volume of the charge cloud collection depends on the depletion region. Typically, there are several types of the photo-diodes with varying applications.

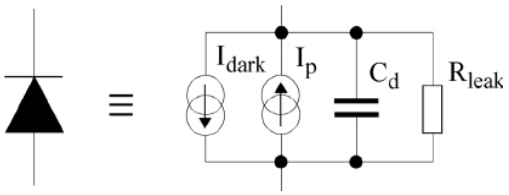


Figure 2.2: Shows the generalization of the photo-diode. The I_{dark} is the current when a photon is present, I_p is the current generated by electron/hole production. C_d is the combined capacitance of the photo-diode, R_{leak} is the resistance of the PN junction.

The focus will be on Avalanche Photo-diodes (APD), since they operate like the main photo-sensors used by the detectors. An avalanche photo-diode is a photo-diode that is optimized to operated when the diode is negatively biased and sensitive enough that it can create an avalanche effect to generate a large charge collection at the anode. They are highly sensitive in the optical range and all photo-diodes typically respond to specific frequencies that increase the number of electron-hole pairs generated. However, unlike the APD, our photo-diode sensor's similarities end at the usage of bias operation due to the source of the electron-hole production. The sensors use x-rays to directly ionize the bulk Si instead of the photoelectric effect. This difference will be apparent as the strip sensor will not have any gain associated with the sensors.

For the previous revision, the main detector used commercially available photo-sensors from a company called Ferminoics. The sensors are made from InGaAs substrates to give them better overall thermal performance. For this iteration, however, we consider a known working design of the strip sensor used in the previously attempted design. The design uses silicon bulk material to increase the recovery timing.

2.1.2 Strip Sensors

Our strip sensor is comprised of highly doped p-type bulk silicon that contacts a series of strips of n-type silicon. The p-type bulk is depleted completely by an external reverse-bias (10V to 75V). The sensors are directly ionized by the incoming x-ray beam and the resultant charge cloud is accelerated by the induced electric field from the reverse-bias, generating the current pulse necessary for detection.

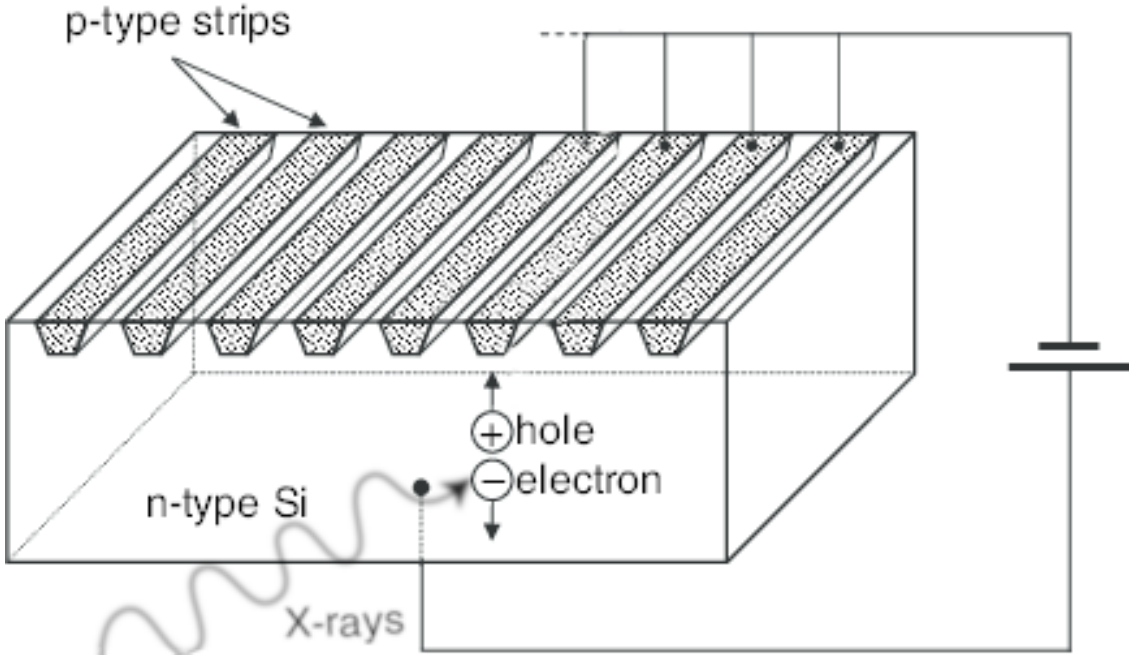


Figure 2.3: Opposite polarity strip sensor (n-type bulk with p-type strips), with x-rays releasing electron/hole pairs, that drift to periphery allowing detection.[12]

The sensor's anodes are surrounded with a guard ring to reduce the noise contribution by the pickup the anodes. The sensors used by the detector will have 128 cathode strips with a pitch of 50 μm. between each other. The design specifically measures the intensity peak from the final mask filter. The sensor's operation requires a bias voltage applied to generate the depletion region. The approximate depletion region for a given bias substrates is given by this equation.

$$x \approx \sqrt{2(\epsilon_{0si})(\epsilon)(V_{bias})(\mu)(\rho)}$$

where ϵ_0 is the vacuum permittivity ($8.854187817 \times 10^{-12} Fm^{-1}$) and the V_{bias} is the applied bias voltages substrate. μ_n is the electron mobility in silicon and ρ is the resistivity of the silicon substrate. Typical bias voltage for strip sensors depend on the thickness of the substrate. Our sensor's nominal thickness is 75um with a silicon resistivity(ρ) of roughly 5kOhm/cm.

The expected electric field in the silicon can be estimated, to first order by the equation

$$E(x) = \frac{2V_{dep}}{W^2}(W - x)$$

where W is the full thickness of the wafer and x is the position inside the n bulk. V_{dep} is the

bias voltage. The maximum potential experienced is when $x = 0$, i.e,

$$E_{max} = \frac{2V_{dep}}{W}$$

.

The desired short current pulse is created due the drift between the electrosn and holes that causes a charge to be induced at the surface. The effect of the diffusion can be neglected if we consider only the ionization of the particle. The appropriate total charge collected is given by the equation

$$\sigma^2(x) = \frac{2kT}{q^2}\frac{\epsilon_{si}\epsilon 0}{n} ln\left(\frac{W}{(W-x)}\right)$$

where, k is Boltzmann's constant, T is the effective electron temperature in silicon, W is the width of the substrate, n is the number of strips and q is the point charge.

Estimate Timing

For a charge cloud that travels, a distance x, the time it takes for the charge cloud to travel between the anode/cathode is

$$t(x) = \frac{\epsilon_{si}\epsilon_0}{n} ln\left(\frac{W}{(W-x)}\right)$$

W is the width of the substrate, n is the number of anodes in the substrate, ϵ_{si} is the permitivity of silicon and the ϵ_0 is the permitivity of free space. For our detector, the substrate is 75μm and we are expecting a maximum time for the charge collection of 5ns. This theoretical value is expected to change depending on the amplifier input's capacitance and the PCB stray capacitance.

Spatial Resolution Limit

The spatial resolution of a strip sensor is given by [8]

$$\sigma = \frac{P}{\sqrt{12}}$$

where, P is the anode's pitchs in meters. The magnitude of diffusion can to some extent be controlled by choosing a very high purity material. The common strip sensor has anode-to-anode pitch of a 20 - 50 μm due to this geometric limit. For our strip sensors, we will have a pitch of 50μm, therefore, our spatial resolution limit is 14.4μm

Strip Sensor Breakout Board

This board was designed by Matt Andrew of the University of Hawaii Manoa and is a breakout board to fanout all 128 cathodes on the SLAC strip sensor to 4 of the mating connectors. The main silicon sensor's pads are wire bonded and epoxied to the breakout board. The breakout board has four ERM8 80 pin connectors that are designed to provide the necessary bias from any connector to the SLAC sensors and to provide four of the high density connection inputs of the preamplifier board. The image of the breakout board is shown in Figure 2.4. The wirebond breakout board was epoxied to the copper block for thermal reasons.

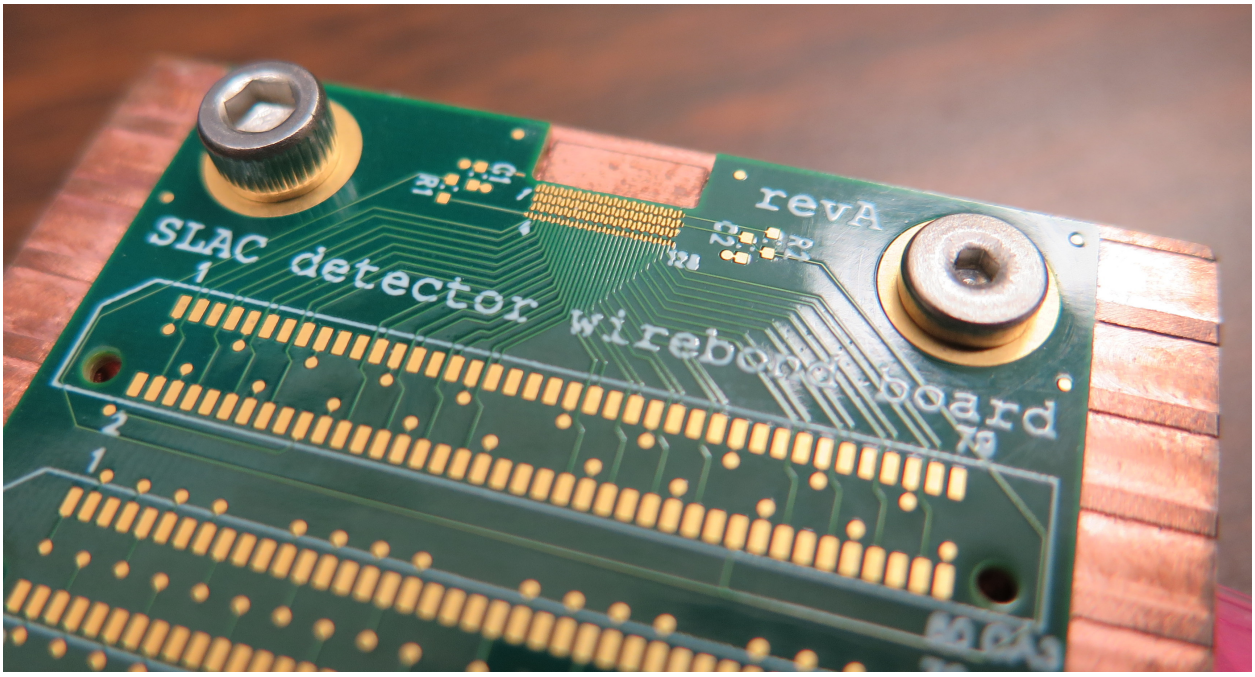


Figure 2.4: Shows breakout board bond pads. 128 anode + HV and HVReturn will be bonded using a bonding wire. The pitch of the PCB bonding area is approximately 4 mils. Designed by Matt Andrew [12]

Further characterization was performed on the sensor. A parametric analyzer was used to create the IV performance varying condition specified in Figure 2.5.

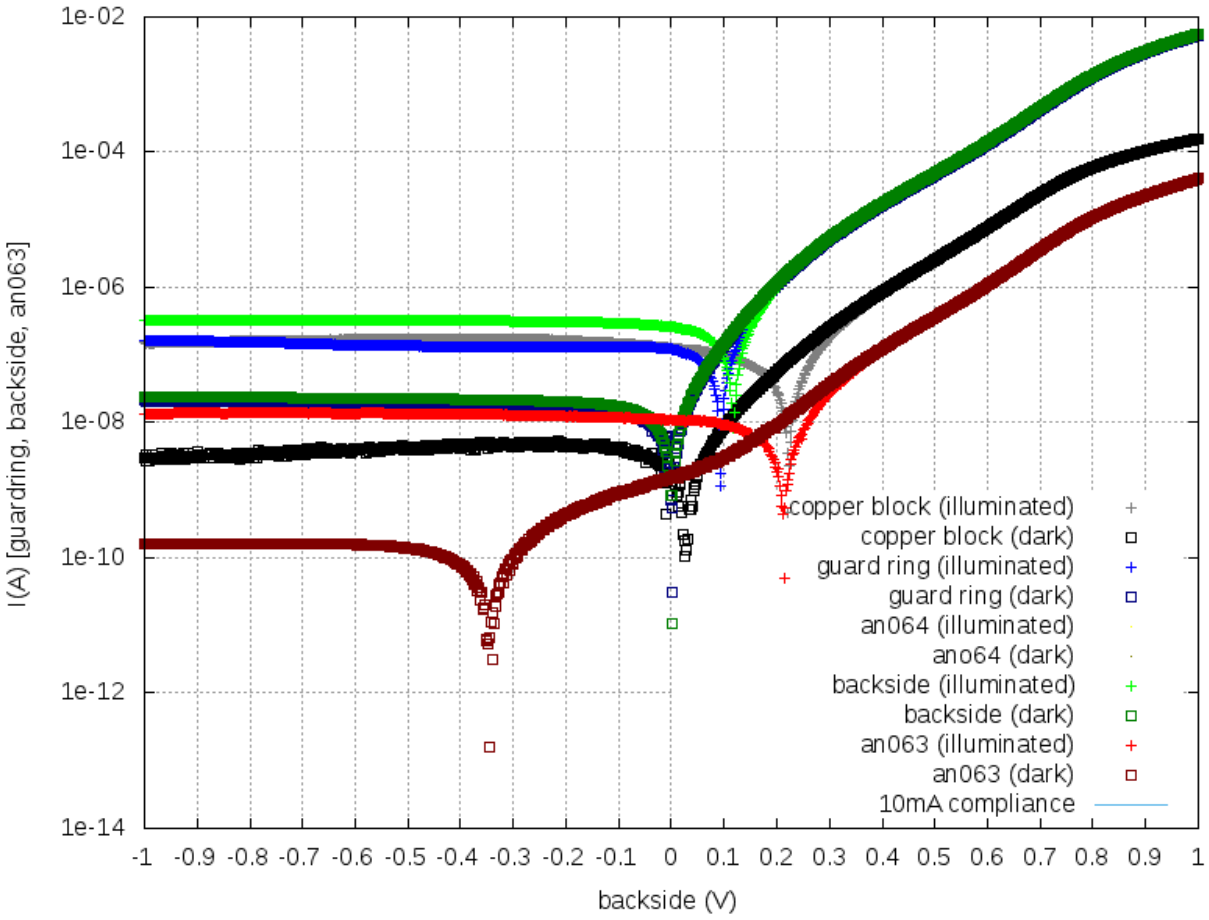


Figure 2.5: Shows the IV curve of the SLAC strip sensors. It shows the IV curve for several conditions such as illuminated and unillustrated while the voltages were swept from -1V to 1V. The IV curve data were taken by Matt Andrew[5]

Using this IV curve and an instrument multimeter (Fluke 287) and LCR meter (Instex LCR-821), the following table for the measured properties of the breakout board sensors was generated.

Characteristic	Min	Max	Summary
$C_{parallel}$	6μF	6.5μF	Measured with LCR from Anode 63 to HV *
$R_{parallel}$	137$M\Omega$	N/A	Slope near the $< V_{IV} >= 0$ @ Dark.
$R_{AnodeSeries}$	291KΩ	N/A	Pin 62 Anode to the HV Backplane. Measured using a multimeter.

Table 2.1: Shows the measured characteristics of the SLAC sensors. Capacitance and resistance measured are the combination of the capacitance and inductance in series and parallel of the breakout board. *Result given here is with no HV bias. We expected lower capacitance when biased (4pF range)

Connector & Pin #	Sensor Pin	Stray Capacitance (pF)	Loss (dB)
CA3-77	128	1.78	0.01
CA2-77	127	3.45	0.63
CA1-77	126	4.77	0.869
CA0-77	125	6.2	1.126
CA0-46	65	6.53	1.182

Table 2.2: Shows the calculated loss associated with the each signal line from the SLAC Breakout board. The loss is significant at Connector 0 due to larger stray capacitance. This stray capacitance is expected to effect the signal's risetime coming from the sensors. Further investigation is needed to determine the maximum rise-time from the sensor.

For thermal reasons, the sensors are epoxied to the board to provide excellent thermal coupling between the FR-4 PCB and the copper cooling block. The 0.3mm grooves with 1mm pitch were milled on the copper block's surfaces so that the epoxy can spread evenly under compression between PCB and the copper blocks. The final sensor assemblies each have a water cooling block mounted to the sensors. Narrow slits are milled (50 mils thin) to act as a window for the beam to strike the sensor.

During the testing phase of the amplifier chains, the sensor's biased was set to -60V using Keithley 6517A, chosen for the low noise output $< 150\mu V_{p-p}$ from 0.1Hz to 10Hz for 100V range[13]. The typical current draw by the sensor was $383\mu A$.

2.2 Read out Electronics

The primary read out electronics are divided into a three main components. A 3D rendering of the detector is shown in Figure 2.6. The components are:

- SLAC Sensor board.
  - The main sensor board. The strip sensors are glued and wire-bonded to the board. It is a fanout for the 128 channel anode of our strip sensors to a SAMTEC ERM8 40 pin board-to-board connector.
- 4x Pre-amplifier stage board.
  - The pre-amplifier stage from our sensors. It has a minimum gain of 20dB. The board is designed to condition the signal before digitization.
- iTOP Boardstack
  - Houses the digitizer boards and communication board. Each boardstack consists of 4 Carrier boards and 1 SCROD. It has 2 fiber optic outputs and an environment sensor on board for operation.

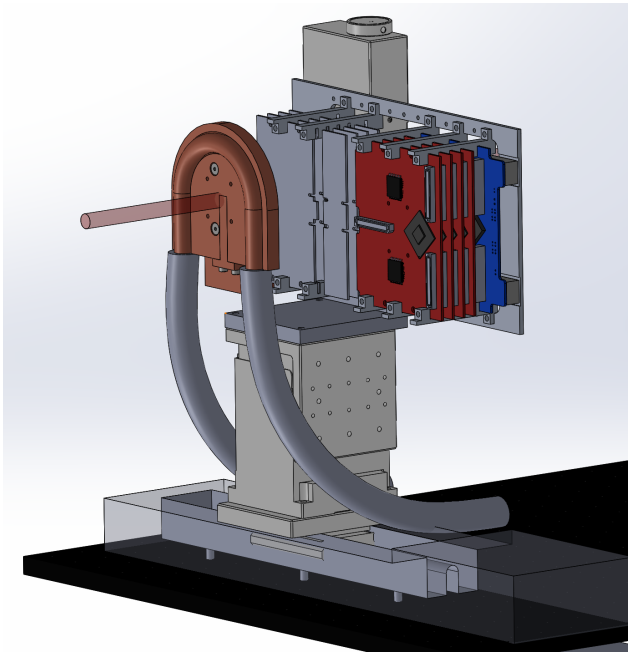


Figure 2.6: Shows the rendered image of the complete electronic read out system.

These electronics and the mechanical structure were designed and built at the University of Hawaii Manoa. This subsection discusses in detail the specifications and primary testing done.

2.2.1 Pre-Amplifier Board

This is a mixed signal board design and the main purpose is to provide the pre-amplification stage before the signal is digitized by the IRSX. The detailed design of the amplifier chain will be discussed in the Chapter 3. The design has a custom built amplifier and also has two temperature sensors on the board, passed through to carrier board.

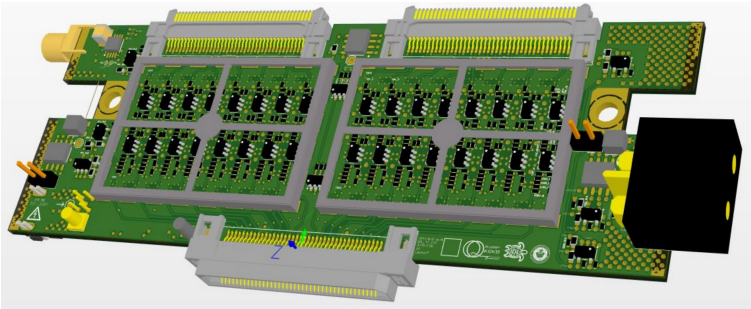


Figure 2.7: Shows the 3D rendering of the preamplifier board. It is a front and back design with an amplifier making each channel as dense as possible.

The custom amplifier chain board has 32 channels per board and a total of 4 boards are required for the complete detector. Each amplifier chain has a minimum gain of 20dB. The amplifier board was designed to allow power to come from the ERM8 mating connectors at the carrier. However, for the purpose of compatibility with older carrier boards, the final design will be powered by an external power supply and regulated down to the amplifier rail voltage. This is primarily due to the current revision of the Carrier board that does not provide the power thought its input connector. carrier Rev E5 is currently being fabricated and should be available for the upgrade to the existing design. One of the main concerns from the last revision is the EMI generated from the klystrons used in the accelerators, coupling to the incoming signal. Detector boxes were not yet built during the previous design, which could provide additional buffer for the EMI. For an extra measured, an RF shield, will be placed over the current amplifier chains to reduce EMI located near the detector box.

The SLAC breakout board requires a high voltage bias connection that is routed through one of the ERM8 connectors. This requires a high voltage (HV) line routed to the connector through the preamplifier board. The current board design provided only a connection to the high voltage to the SLAC breakout boards, and with strict low noise requirements on the HV rail. The design requires high frequency noise filters before reaching the SLAC breakout board. A HV LC low-pass filter (maximum voltage of 350V) on board the preamplifier (20KHz at 3dB) is designed and placed before the breakout board. One of the reasons for these extra precautions on the HV line is because they are the bias voltage pads and each cathode on the strip sensor is AC coupled, thus, it is critical for the ripple going into the sensor be minimized to prevent false positives. The HV rails will be

provided externally through the board with a shielded two-pin connector for additional protection from ElectroMagnetic Interference (EMI).

The board is designed with an external trigger output (SMA Connector), that has two amplifier outputs connected to an RF multiplexer, to be used as an external trigger for a software trigger on the IRSX.

2.2.2 Ice Radio Sampler Revision X (IRSX) Digitizer ASIC

IRSX is an Application Specific Integrated Circuit (ASIC) that was developed at the University of Hawaii by Dr Gary Varner. The ASIC uses a Wilkinson ADC structure to digitize signals.[17]. The specification of the digitizer is shown in Table 2.3.

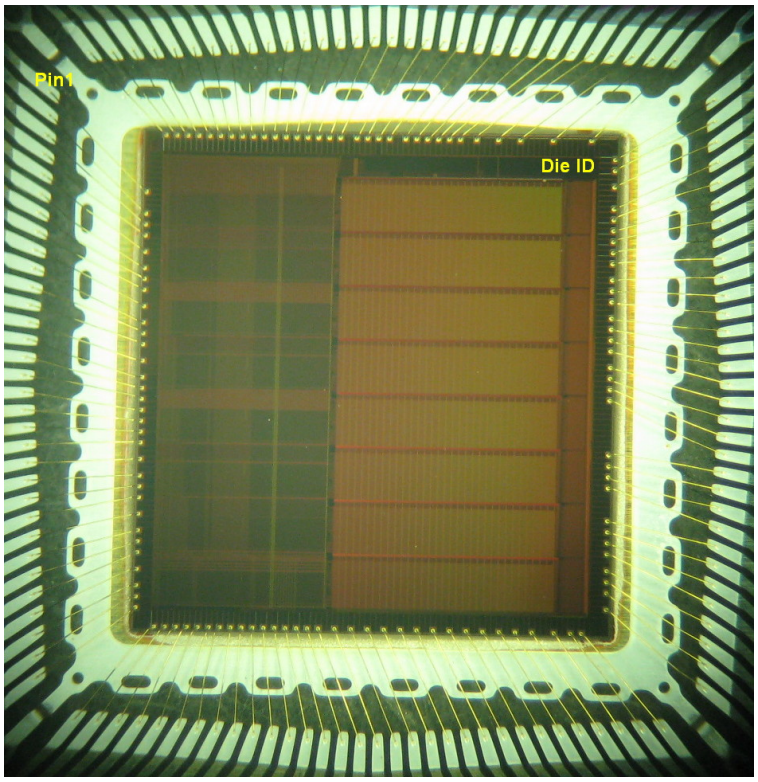


Figure 2.8: Shows the IRSX die image after wire-bonding into a TQFP-128A Package

Sampling rate	4GSa/s
#Samples/Window	64 (16 ns)
Read out Rate	up to 100kHz
Storage Per Channel	512 Windows
Input Termination	50Ω
#Channel	8

Table 2.3: The specification of the IRSX

The digitizer can accept an input voltage range from 0.5V to 2.0V and will be used as the main digitizer for the signal coming form the amplified current pulse.

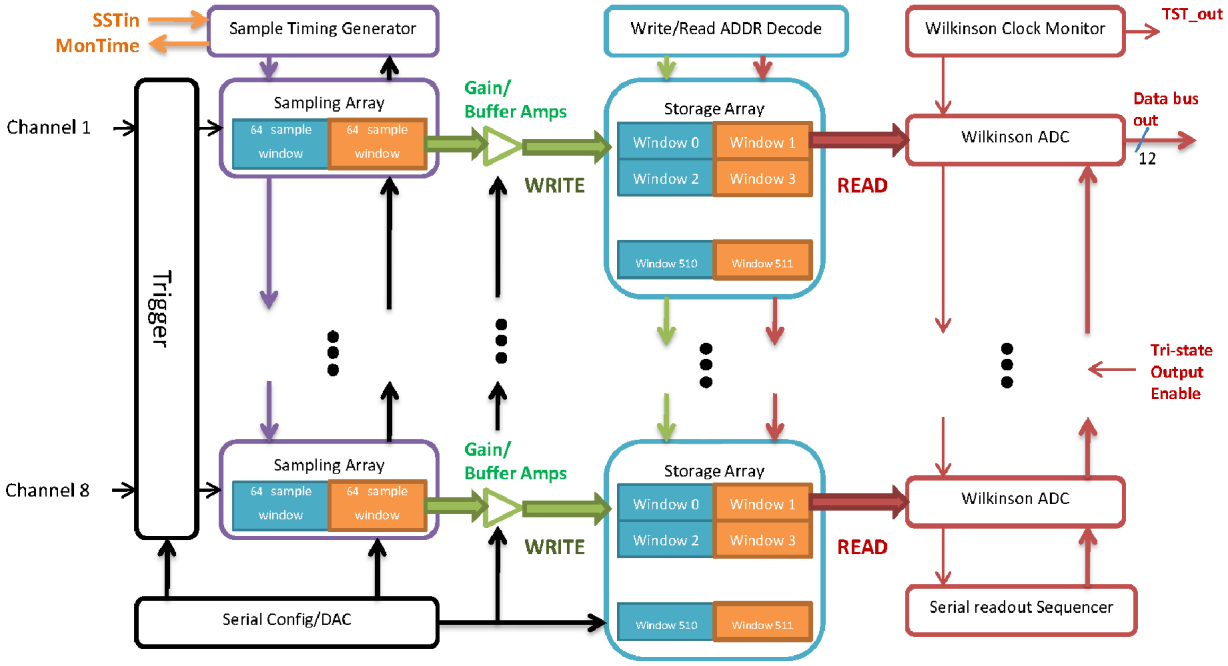


Figure 2.9: Shows the IRSX functional diagram.

The roll-off of the IRSX analog bandwidth is approximately 700MHz. Data streams are in 16 bit serial stream ports to increase the read out rate of the IRSX. The main benefit over the conventional ADC is the number of channels and the reduced total power consumption, with typical power usage being 400mW (dependent on number of digitization.)

2.2.3 Carriers

The modified carrier Rev E3 is used as the main ADC board for the detector. The purpose of the carrier board is to digitize signals from the preamp and output digitized waveforms. On board the carrier, there is an initial LMH6629 amplifier which has the gain set to 20dB in an inverting configuration. The carrier provides the amplifier stage needed for the IRSX ASIC. It has 4 ASICs on board and a Zynq XC7Z0200 FPGA that is used control the 4 IRSX and the DAC, to set the voltage pedestal for the amplifier stage.

Each carrier board can be stacked with three of the mezzanine connectors located at the bottom of the boards that provide power and a signal path for carrier. The carrier is designed to be dependent on the SCROD for power and control, except for the three header for power and 4 pin JTAG, which can be used for debugging purposes and requires soldering a wire to provide external power.

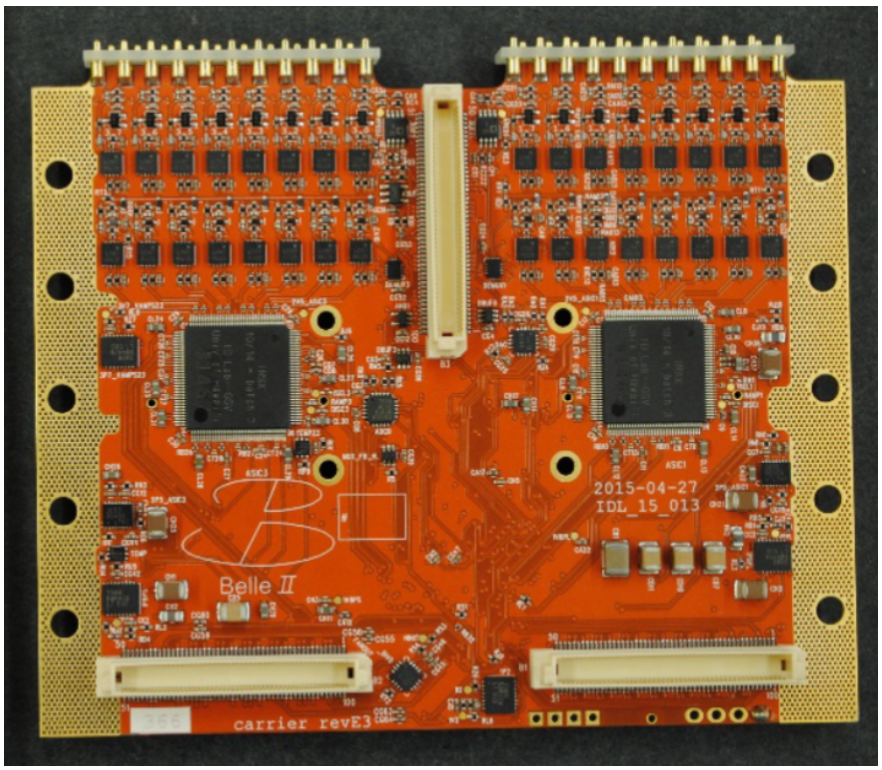


Figure 2.10: The image of top view of the Rev E3 version of the carrier. For the XRM, pogo pin that were used in Image Time Of Flight Detector, is replaced with a SAMTEC Edge-Mounted Connector (ERM8) to be compatible with the amplifier board.

The carriers were designed to be stacked on top of each carrier, and for can potentially be stacked up to increase the number of channels to 128 per each SCROD. The carrier requires the SCROD to be read out from the Belle II Link. The carrier also has three on board temperature

sensors to monitor different sections of the board. For applications with XRM, the Carriers input pogo pin connectors have been modified to accept the ERM8 Female Connector that comes from the amplifier board.

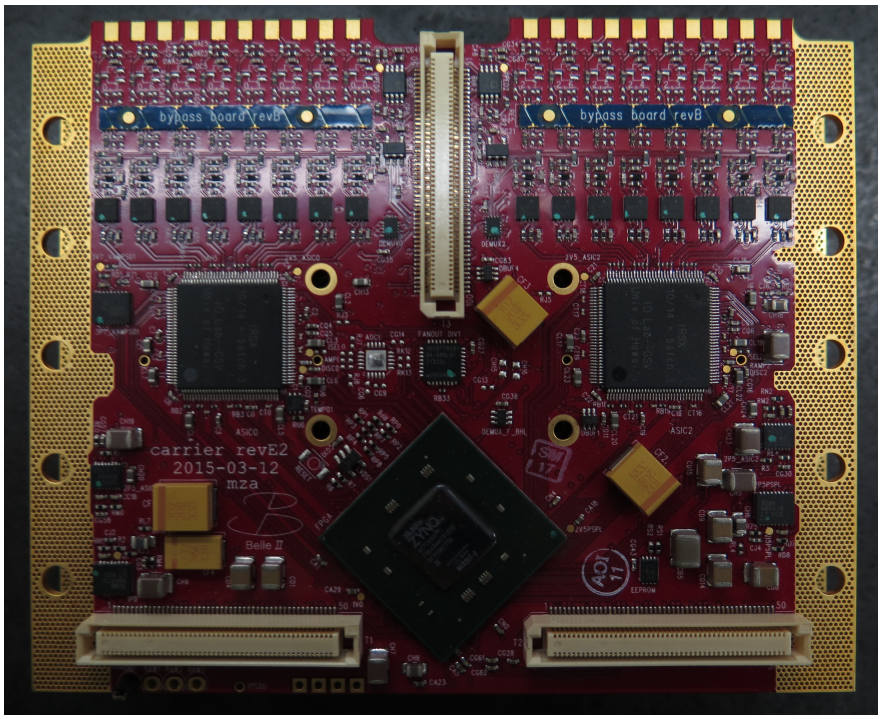


Figure 2.11: Image of modifications done to the carrier board. The first amplifier were by-passed by a custom PCB boards and only the second stage amplifier remains in an inverting configuration.

For use with the XRM, I2C is rerouted through the ERM8 Low-Density connector to control the temperature sensor and the multiplexer on board the preamplifier. Modified iTOP firmware will be used for XRM since trigger mechanisms are similar. The only change will be window size of each event to be smallest possible on the IRSX, to capture all of the bunch events.

2.2.4 SCROD

The Standard Control Read-Out Data (SCROD) Rev B2 is the main communication board between carriers and PC. The board was designed by Matt Andrew for the purpose of controlling the carrier boards, for the iTOP sub-detector at Belle II. It houses a Zynq 70045 FPGA which has two ARM core process on top to do complex operations such as a pedestal subtraction, feature extraction, or implement a Gigabyte Ethernet protocol for data retrieval purposes.

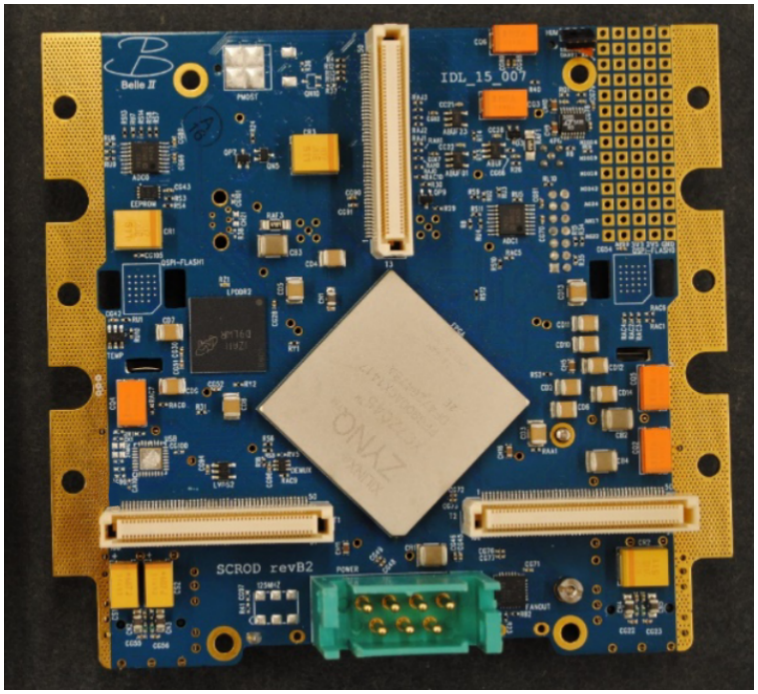


Figure 2.12: Shows the Rev E4 version of the SCROD Rev B2, image taken by Dmitri Kotchetkov[18] The top layer shows the two metal case for the fiber optic, the bottom view, shows the FPGA and the 3 mezzanine connector that connects to the carrier board to communication and power.

The board has two fiber-optic connectors for transmitting and receiving data and trigger information. The board also uses a custom connection called Trigger and JTAG hooker Rev A (also known as "T.J. Hooker") which can be accept a Gigabit Ethernet RJ45 Connection, for the purpose of receiving external clock and JTAG information. The SCROD's is primary goal is to manage data coming from the carriers. A total of four carriers can be attached to the three mezzanine connectors on board the SCROD and when they are stacked are typically referred to as a "boardstack". This boardstack is a complete read out system with the ability to change configuration depending on the application. The boardstack requires three LV power rails for operation (2.5V, 3.3V, 4.0V) and is connected though a Positronic connector. The boardstack can be cooled using air or a heaksink with a water-block. For the XRM application, cooling of the boardstack is done with a 12V DC fan located inside the detector box.

2.2.5 X-ray Timing Distribution (XTD)

The XTD is a NIM module designed at the Unversity of Hawaii Manoa for the XRM system. Revision A of the board was designed by Khanh Lee and the current revision was designed by the author. The purpose is to distribute the revolution marker of the particle bunches as a trigger, fanout system clock coming from accelerators, and remotely program the boardstack.

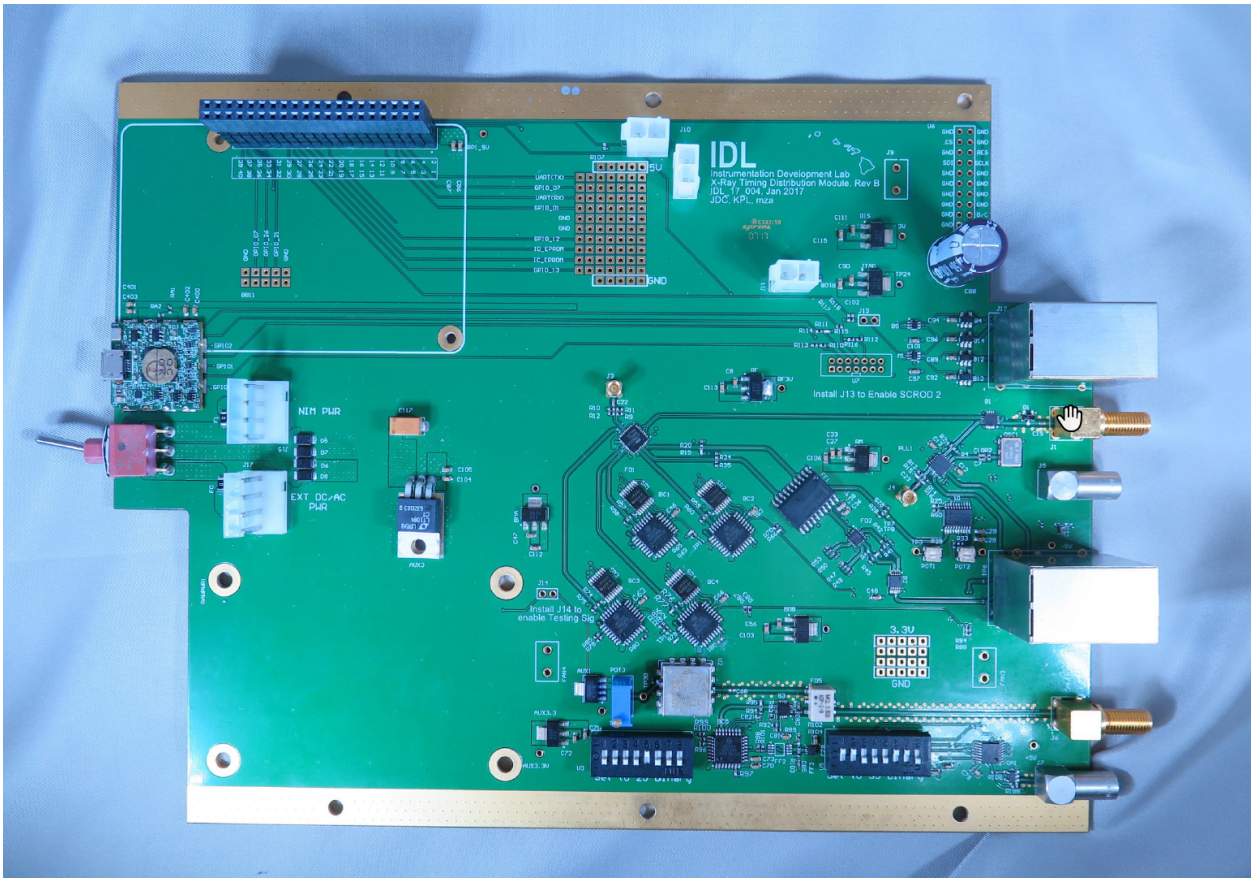
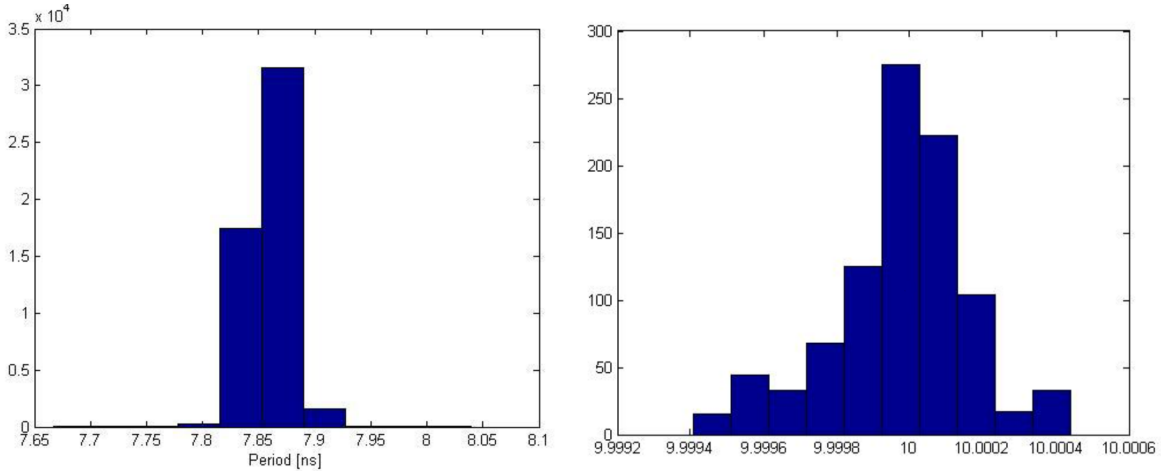


Figure 2.13: Show a fully populated XTD Board Rev B. It uses a Raspberry Pi 2 SBC to control the output and to select the number to divide the global clock signal (508MHz) to the local system clock (127.15MHz).

It uses an internal PLL to phase lock the global clock accelerator to sync the revolution marker to the global clock edge and also down-clock and regenerate the global clock. All signals are output to two RJ45 connectors and the connection is wired to the boardstack, where it will be used as a global system clock. The jitter performance of the clock is critical for this application and was measured. The histogram of the jitter performance is shown in Figure 2.14.



(a) A system clock's jitter

(b) A revolution marker's jitter

Figure 2.14: Shows the jitter performance of the synchronized system clock (127 MHz) and revolution marker (100 MHz). The average jitter for system clock was measured to be 18.75 ps. [9]

The module also has VCO tuned to 508MHz SMA to simulate the Super-KEKB global clock on the board, for verification of the revolution marker generation and synced clock output.

2.3 Power Supply

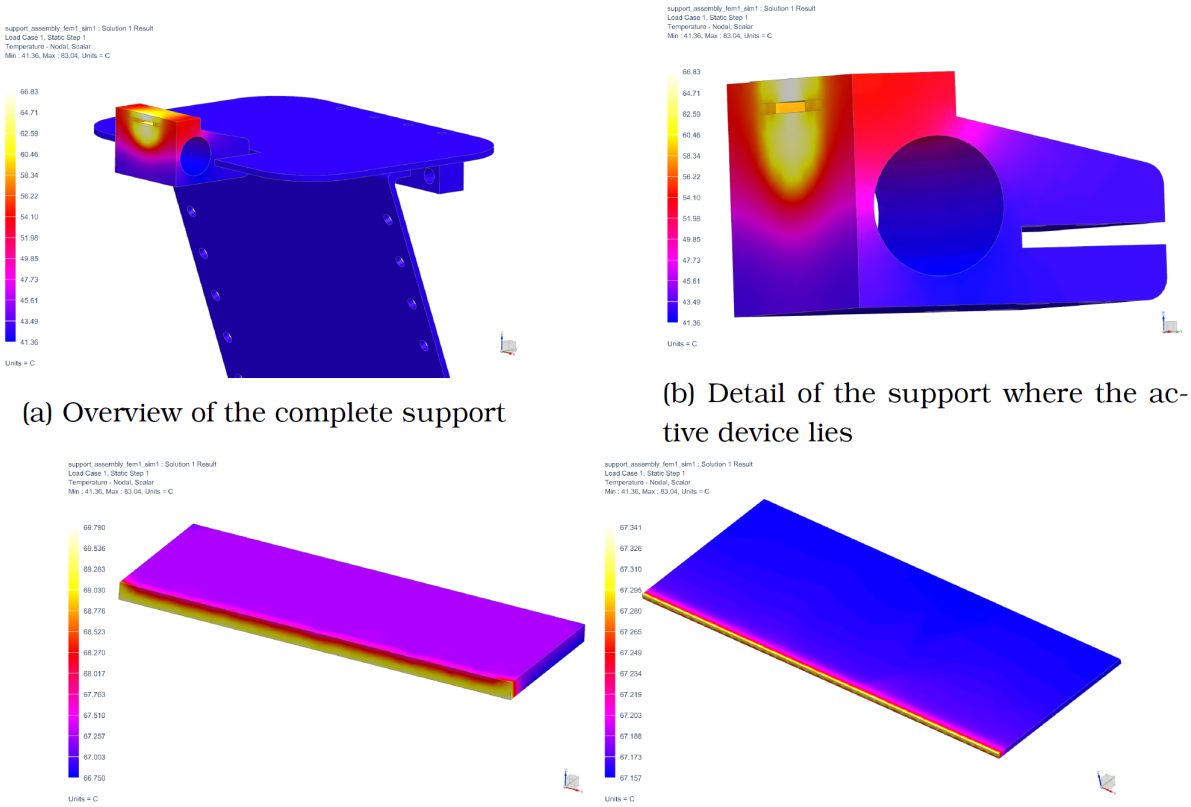
For the low voltage supply portion of the detector, Excelsis Low Voltage Power Supply is used to supply all the necessary voltage. The power supply is capable of operating four LV modules for powering all of the XRM, the boardstack and the pre-amplifier board. All boards have an on board regulator. The low voltage does not require strict consideration. The low voltage only requires the capability to provide the current for the board stack and preamplifier board.

For the High Voltage (HV) Rail Supply, we need to be careful as it directly influences the noise at each sensor's anode, due to the small expected signal to noise ratio (SNR). The bias voltage has been AC coupled from the sensor's anodes. The HV supply provides bias for the sensors, therefore the bias voltage output noise and ripple must be constrained to give an ad-quite chance for detection. In the worst case scenario, The sensor's load is expected draw a $\sim 1\mu$A current, therefore the current draw is difficult to find. A smaller/compact HV supply, such as the DRV8662 evaluation board (1% noise + distortion) or HV ultrasonic modules ($\frac{26\mu V}{\sqrt{(Hz)}}$) were initially considered due to the low noise output, however, all exhibit a high ripple output that could not be trivially removed by a low pass filter applied on its output. For the testing done at the IDLAB and at the photon factory, we will be using a Keithley 6517A HV power supply.

2.4 Thermal/Mechanical

2.4.1 Rotating Arm Mechanical Design

The current detector mechanical design incorporates the entire electronics read out to be mounted on a SPSG33 Sigmakoki, in order for sensors to sweep across the synchrotron beam. Due to the beam power, the sensors will be exposed to sudden increases in temperature that could cause damage without cooling. The initial strategy considered using diamond backing for use as a cooling substrate however, the initial assessment of the thermal simulation done on the current mechanical model by Fransisco Fabio showed that copper blocks with liquid cooling are capable of cooling the sensors with a reasonable operational temperature of 66°C when the exposed to a $\sim$300W Gaussian beam source.



(a) Overview of the complete support

(b) Detail of the support where the active device lies

(c) Detail of the silicon wafer

(d) Detail of the sensor

Figure 2.15: Shows the Thermal simulation of the made by Fabio Rinaldo. The temperature gradient is shown with max temperature of 66°C [11]

The temperature will be monitored by the temperature sensor on board the amplifier board, to provide the feedback information regarding the current ambient temperature inside the detector box and the sensor proximity. The current revision of the mechanical structure was designed to have all electronics mounted to single aluminum 6080 frame, by 2x2.5M screws, designed to be easily detachable from the cooling and rotational arm.

2.5 Specific Contributions to the XRM

The author's specific contributions to the XRM project are highlighted in Figure 2.16. The two main contributions are the XRM Timing Distribution board (XTD) and the amplifier design. Specifically, XTD includes designing, populating, and measurement of the jitter performance. The primary discussion of this thesis is based on the amplifier designs and requirements. The author's contributions include the design, simulation, and testing of different amplifier chains that potentially satisfy the XRM requirements.

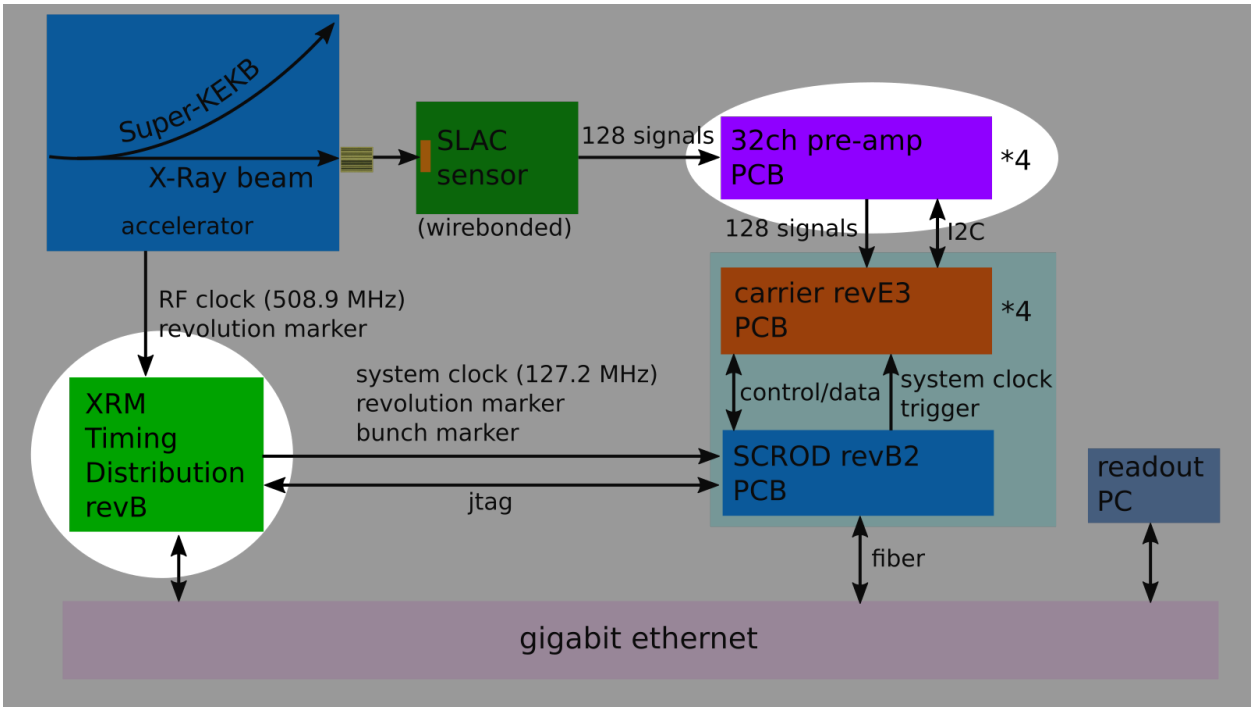


Figure 2.16: The highlighted regions indicate the specific components of the XRM system that are the author's contributions.

CHAPTER 3
DESIGNING A NEW AMPLIFIER CHAIN BOARD

3.1 Amplifier Board Design Considerations

The design requires mating with the existing boardstack design. There are several physical constraints on the amplifier design that needed to be considered during the design process. Each section will cover in detail such restrictions placed on the current design. After covering the each issue regarding the amplifier chains design constraints, the test board used to evaluate each amplifier chains and the current design for multi-channel version of preamplifier to boards, is discussed.

3.2 Amplifier Selection

Choosing the right amplifier for the new revision of the XRM is critical for its operation. From the previous revision, it was learned RF Low Noise Amplifier(LNAs) cannot be applied with the strip sensor due to a baseline issue. This may have been an issue with a termination mismatch. Whatever the case, we would need to find a alternative amplifier. A list of constraints were created to better qualify the needs for this particular sensor. These criteria do not need to be on all of the stages on the amplifier design, since overall-performance is evaluated. owever, it will be used as a guideline for amplifier selection. The list of critical design parameters is given below.

1. DC coupled amplifier.
2. Can handle bandwidth up to 750 MHz.
3. Physical package cannot exceed 3.4mm in height (due to physical collision with the Top/Bottom boards).
4. Requires high slew-rate (Minimum: 1V/ns).
5. Total minimum gain are 20 dB (overall Gain)
6. Each amplifier maximum current draw must be $\sim$ 30mA
7. Single supply voltage 3.3V – 5V (commonly available voltage) or dual supply (need additional rails).
8. Lower input reference noise ($< 1.5nV/\sqrt{Hz}$)
9. Commonly available from distribution(distributers: Digikey and Mouser).
10. SOT23 package or other easily hand-solderable package.

The first requirement was due to the previous detector design having an issue with DC baseline. The current consensus is that a DC coupled input will help return to baseline faster than an AC coupled version. Alternatively, if the capacitance used to AC coupled is small, there will be enough value to return to baseline faster, which will be explored in one of the amplifier designs. The IRSX requires an input voltage range around $1.25 \sim 2.5$Vthus, the final stage output of the amplifier needs to be AC coupled and provide a voltage pedestal for proper ASIC operation. The second criteria is due to the expected beam bunch time intervals. Although a previous stage of development had the particle bunch spacing larger, the final design requires the spacing to be on the order of 2ns and the expected current pulse's rising edge is expected to be on the order of 500 picoseconds. Thus, We would need to be able discern a fast rising edge pulse with a relatively fast event rate.

The package height is restricted due to the spacing between the existing digitizer module electronics, which has a board-to-board clearance of 7.0mm. This restricts the overall height of the selection for shielding/package of amplifiers to 7.0mm/2 = 3.5mm. The current design requires top and bottom channels to be mirrors, to maximize each channel density on board, thus the total is divided by two from the total spacing available. The fourth requirement on the list is necessary to prevent tails and the next bunch from overlapping. The tails formed at the end of the output signal because the amplifier slewrate is not fast enough to return to the common mode voltage at the input. If the signal overlaps due to the fast event rate and high gain, it will cause the baseline to change, defeating the purpose of this revision. The fifth requirement is given for a gain requirement on the preamplifier design The first and second stage amplifiers do not require it to be high gain. However, the initial stage was selected to be higher gain than the predictor stage to reduce the noise contribution.

3.2.1 Amplifier Choice

To narrow down the choice of amplifiers, a table of potential amplifiers is created. If the amplifier in question meets the three of desired properties, the amplifier is nominated to the list. The complied list of amplifiers candidates is shown in Table 3.1.

	Part Name	Architecture	-3dB	$I_{typical}$	Slewrate	g_{min}	$\frac{nV}{\sqrt{(Hz)}}, \frac{pA}{\sqrt{(Hz)}}$	V_{supply}
1	LMH6629	SiGe VFOA	1GHz	15.5mA	1600V/us	10*	0.69,2.6	$3.3-5.0, \pm 1.7-3.3,$
2	THS3202	SiGe CFOA	2GHz	30mA	9000V/us	1	1.65,13.4	$6.0-12V, \pm 3.3-7.0$

Table 3.1: shows the narrowed-down amplifier candidates for XRM. *Fixed gain, compensation is required to lower gain.

The final amplifier decision was made due to both LMH6629 and the THS3201/THS3202(dual package) having a SPICE model available and a wide selection of packages including SOT23-5.

3.3 Amplifier Chains

The following two designs were selected using all of the previous constraints listed. There are three different types amplifier chains that have negative and positive aspects. First, chains design used two LMH6629 amplifiers; one in non-inverting and the final stage being inverting stage with a total gain of 110. The design goal was to achieve the lowest noise and lowest power. The second amplifier design uses a 2x THS3202 CFA amplifiers both in non-inverting configuration, with the gain 20. It uses the highest performance amplifiers to achieve the highest bandwidth possible. The final amplifier design incorporates both LMH6629 and THS3201 amplifiers into a single design. It uses a non-inverting configuration on the first stage and the second stages are inverting for this configuration. LMH6629/THS3201 is a balanced approach to achieve lower power consumption while giving higher bandwidth. All amplifier designs use non-inverting configuration to provide the widest bandwidth possible for the first stage, while second stage gives additional amplification. An example of a SPICE simulation used to simulate the amplifiers is shown in Figure 3.1.

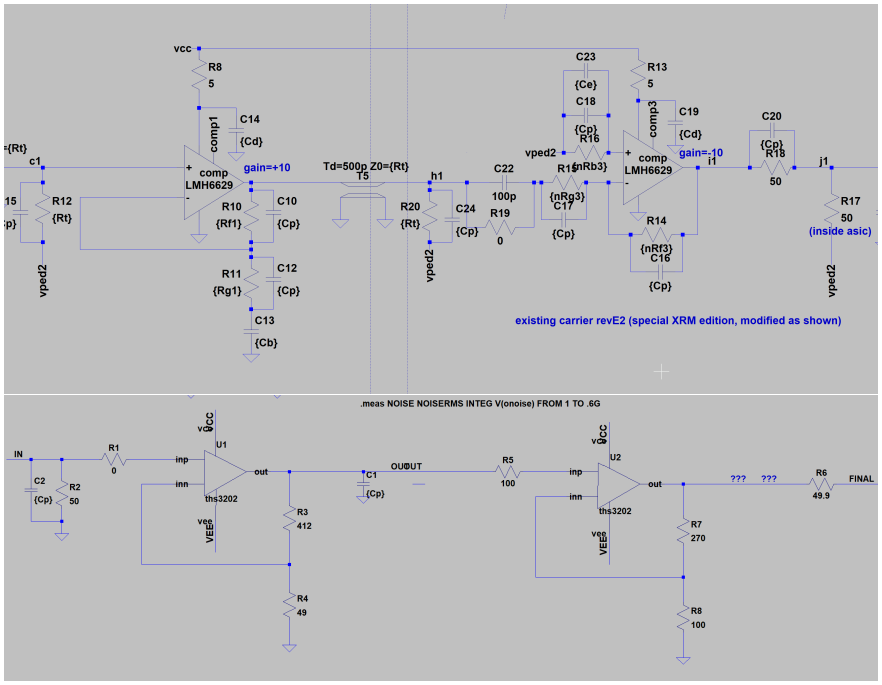


Figure 3.1: The SPICE schematic of the amplifier chains used to simulate the circuit. SPICE software used was LTspice. Top view shows the configuration for non-inverting/inverting configuration and the bottom shows the non-inverting/non-inverting configuration.

3.3.1 Board Design

Board Shape Considerations

Since the board is mounted to a rotating body, the physical PCB with the pre-amplifier requires to be compact and weigh less than its predecessor. The SLAC breakout board is mated with the amplifier board and uses the Samtec Edgefire 80 pin connector and the carrier board has been modified to have a 100 pin version of Edgefire connectors board to board as a connection. The final design for this board is required to be 108 mm by 56 mm and uses Samtec's Edge-rate connectors, allowing analog and digital signal passing between the board to boards. Unfortunately, we are required to route the HV ($60 \sim 75$ V) bias through the connector operation of the SLAC sensors. This requires additional considerations for the keep-out area for the HV line.

Layout Considerations

For the board layout, the costs of manufacturing and the RF routing were considered. The board is a four layer design and uses a single power plane and single signal layer to bring down the cost. Opting to use a commercially available connector instead of using pogo pins made the design more compact than its previous revision. By decreasing the signal path for each channel, the new revisions reduce the loss due to the dielectric substrate. Since the input of the IRSX is impedance matched to 50 Ω, the traces are required to be matched. The final stage of the amplifier traces (the micro-strip and the stripline) are designed to be set to 50 Ω.

To simplify the connection needed, the following naming convention was made regarding the board-to-board connection. The input and output had two names: high and low-density side connectors. The low density side connections are on the digitizer board side and consist of the amplifier's output, and provide digital access to the on board temperature sensors. Both high-density and low-density connections use the same connector: Samtec EdgeRate 80 pin male connector, for connection with the sensors breakout board and the digitizer board. The connector has a low contact resistance ($330m\Omega$) and a low profile making it ideal, since the digitizer board-to-board pitch is 7.0mm. For both types of connections, the pinout are shown in appendix C.1 and C.2.

The amplifier feedback loop is recommended to have no copper pour under the feedback loop to prevent stray capacitance from phase shifting, since the pole is determined using

$$f_p = \frac{GBWP}{2\pi R_f C_p}$$

where GBWP is the gain bandwidth product of the amplifier, R_f is the feedback resistance, and C_p is the stray capacitance of the board/component.

Noise Considerations

For the pre-amplifier stage to be successful, it is necessary to lower the noise contribution seen by the IRSX digitizer. The SLAC sensors introduce considerable noise to the overall system: dark current (I_d), thermal noise (e_n) and shot noise from parasitic resistance. These contributions need to be considered, however, the dominant noise contribution is not from these factors but the amplifier input reference noise, termination resistor and current noise (only in current feedback configuration). The board that is mated to the breakout board must be designed to minimize noise contributions during its operation.

In order to minimize their effects, the sources of all potential noise must be minimized. There are several noise sources that need to be consider when designing the amplifier board; The amplifier input reference noise, the mismatch in the transmission line, input termination Johnson's noise, and possible coupling from EMI.

The amplifier input reference noise can be minimized by careful choice of amplifiers. The mismatch is difficult to manage since the sensor's impedance is currently not known when it is biased. However, the board is designed to be 50Ω for all of the traces leading up to the amplifier and termination value that limits the voltage generated. Input termination is the primary method to convert the current that coming from the sensors to voltage. The design requires Johnson's noise introduced from the termination resistor. The noise contribution from termination resistor is relatively small, however if one haphazardly selects a resistor to be of high value to increase gain, the resistor can end up introducing more noise into the system. There is a trade-off in terms of selection of the higher termination resistors for higher voltage gain and noise at the input.

The detector's anodes are AC couple to each other and could cause crosstalk to occur on the near by channel inputs. The leakage current (dl_{dleak}) from the strip detectors are constant and is a sum of ripple from the HV supply current noise (dI_{HV}), plus noise from the amplifier/termination. If the goal is to have the lowest noise from the anodes, we need to select an HV supply with lowest output noise/ripple.

3.3.2 Simulation Using SPICE

Most of the amplifiers under consideration were commercially available. SPICE models for each of the amplifiers were provided by their respective companies. SPICE is used to validate the expected result and used as a initial comparison. The simulation of each amplifier's input is stimulated using an expected output from the sensors. Using the expected output from the SLAC sensors, a transient analysis was performed to determine the performance of the amplifier chains. Figure 3.2 shows the input signal used during the transient simulation.

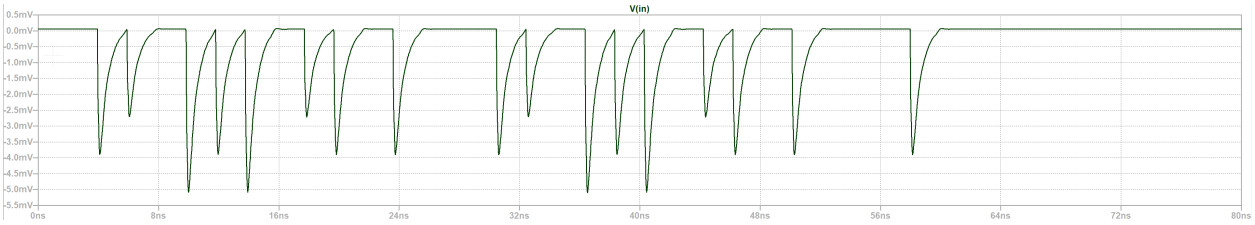


Figure 3.2: Shows the transient simulation test pattern. These pulses are generated using an expected pulse shape from the strip sensors.

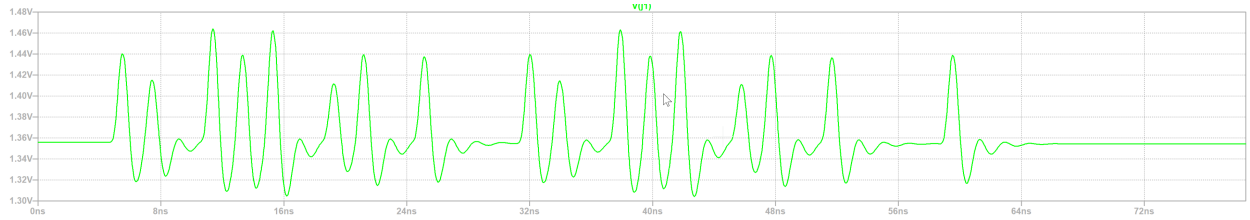


Figure 3.3: Shows the transient simulation result for amplifier chains with two LMH6629 in series. Supply voltage is set to $+3.7V$. The rise-time was measured at the final stage of the amplifier.

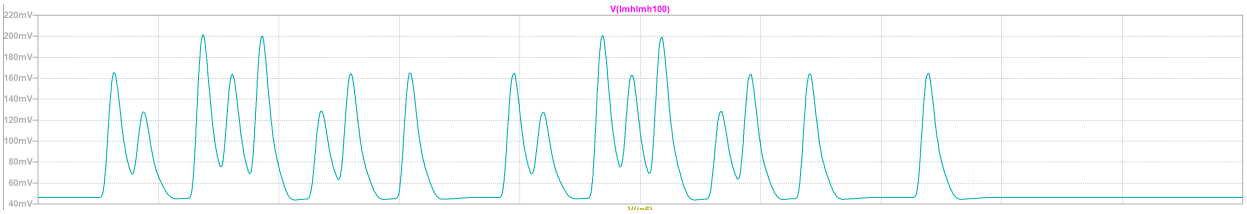


Figure 3.4: Shows the transient simulation result for amplifier chains with two LMH6629 in series. Supply voltage is set to $\pm 2.5V$. The rise-time were measured at the final stage of the amplifier.

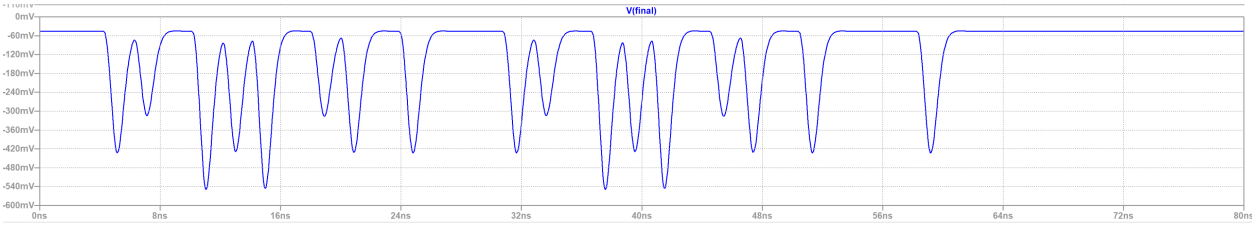


Figure 3.5: Shows the transient simulation result for amplifier chains with THS3202 in series been simulated. Supply voltage is set to $\pm 3.7V$, expected rise-time is 520 ps.

The simulation with the Little Amplifier Board, with combination of THS3201 (Single Channel version of THS3202) and LMH6629 is shown in Figure 3.6

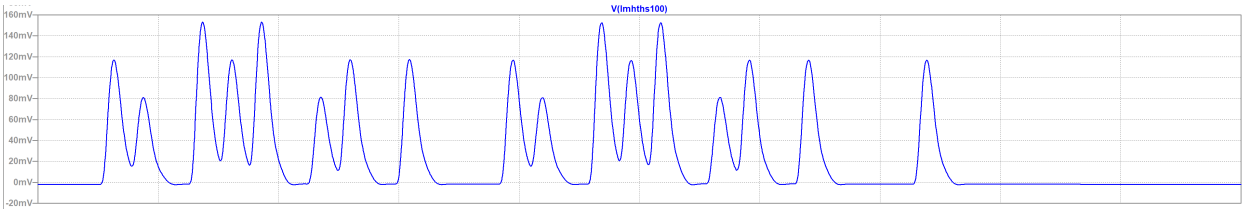


Figure 3.6: Shows the transient simulation result for amplifier chains with LMH6629 and THS3201 in series. Supply voltage is set to $\pm 3.0V$. Expected rise-time is 474 ps.

The AC analysis was performed to determine the -3dB point of the amplifier design. This value is used to analyze the measurements gathered by the network analyzer. Each of simulated circuit results has three plots. The top plot shows the input band, second is the signal trace of the first amplifier's output, and the last shows the final output. The AC analysis on the LMH6629 version of the amplifier chains is shown in Figure 3.7

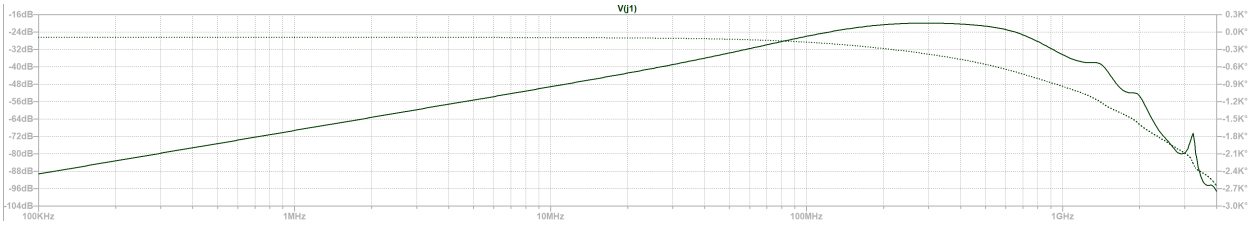


Figure 3.7: Shows the AC simulation result for amplifier chains with LMH6629 in series being simulated. Gain : 20 and -3dB : 500MHz. Supply voltage : +3.7V. Single supply requires to be AC coupled for operation.

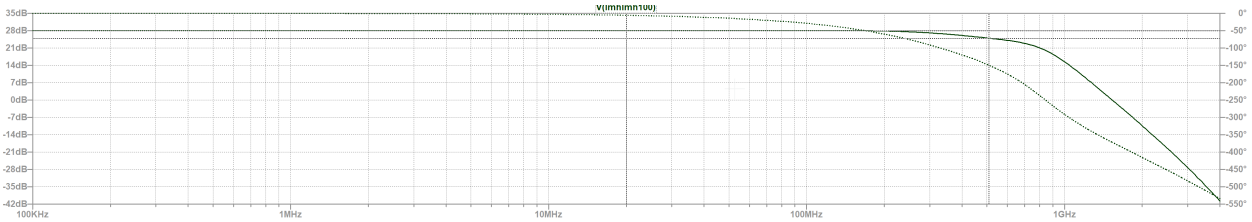


Figure 3.8: Shows the AC simulation result for amplifier chains with LMH6629 in series being simulated. Gain : 28dB and -3dB : 500MHz. it is the same as the single supply amplifier. Supply voltage : $\pm 2.5V$

The AC analysis for the THS3202 version is shown in the Figure 3.9.

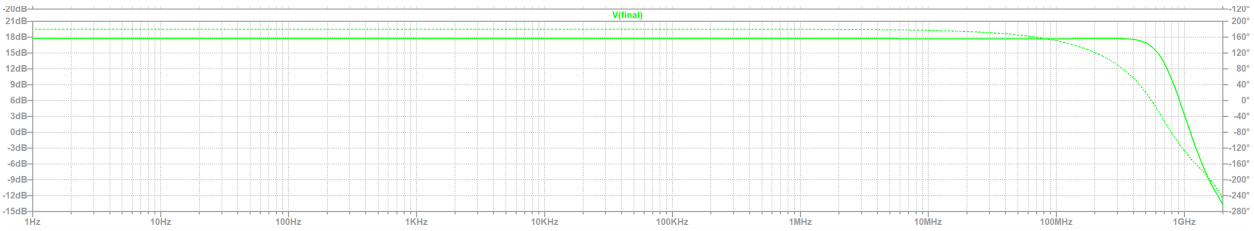


Figure 3.9: Shows the AC simulation result for amplifier chains with THS3202 in series. Gain : 20 and -3dB : 627MHz

For final design, LMH6629 and THS3201 were simulated and their bode plots, shown in Figure 3.10.

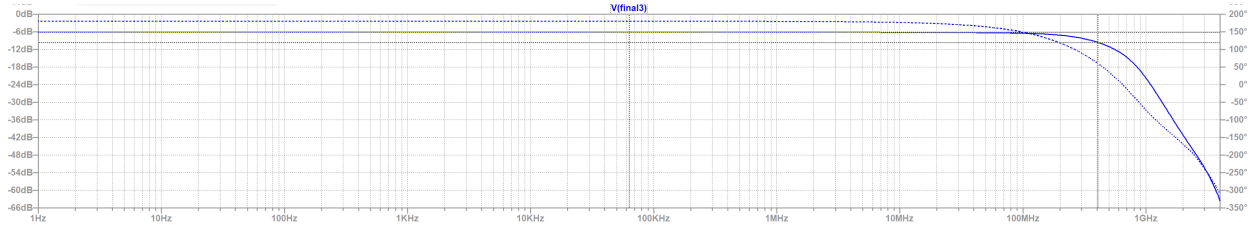


Figure 3.10: Shows the AC simulation result for amplifier chains with LMH6629 and THS3202 in series. Gain : 110 and -3dB : 460MHz

The noise analysis was performed on the existing amplifier design. The expected result from the simulation is compared to the final measured results The expected result was integrated over the expected bandwidth of the amplifier. For this case, it is assumed that it is bandwidth limited to 600MHz for all of the simulation, Figure 3.11 - 3.14

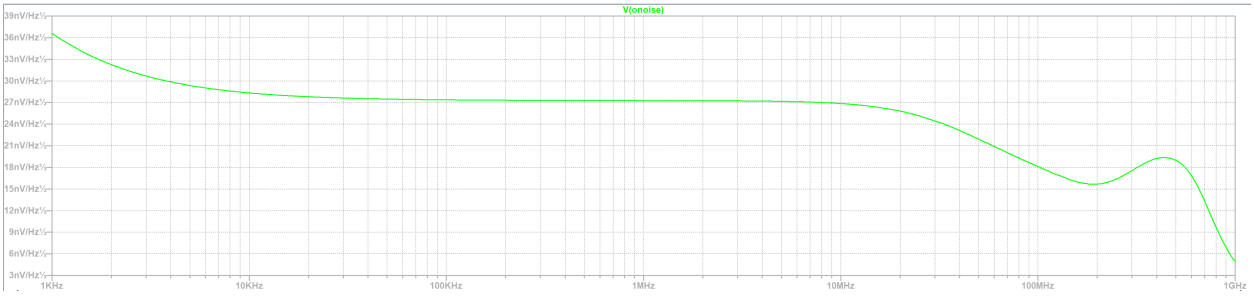


Figure 3.11: Shows the noise simulation result for amplifier chains with LMH6629 on the Little Amp Board. $V_{rms} = 457\mu V_{rms}$ Supply voltage : $+3.7V$ at BW 1Hz-0.6GHz

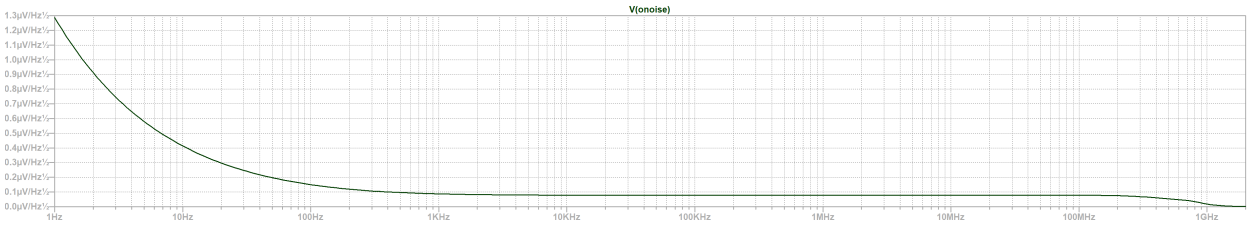


Figure 3.12: Shows the noise simulation result for amplifier chains with LMH6629 on the Little Amp Board. $V_{rms} = 475\mu V_{rms}$ Supply voltage : $\pm 2.5V$ for at 1Hz-0.6GHz

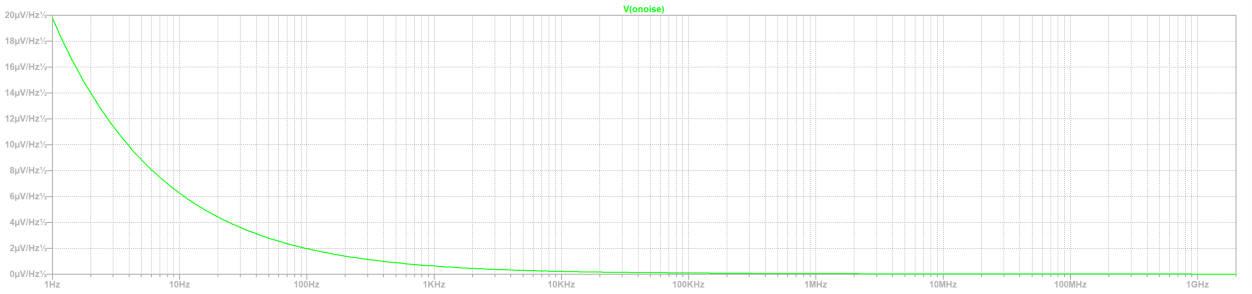


Figure 3.13: Shows the noise simulation result for amplifier chains with THS3202 in series. $V_{rms} = 829\mu V_{rms}$ at BW 1Hz-0.6GHz

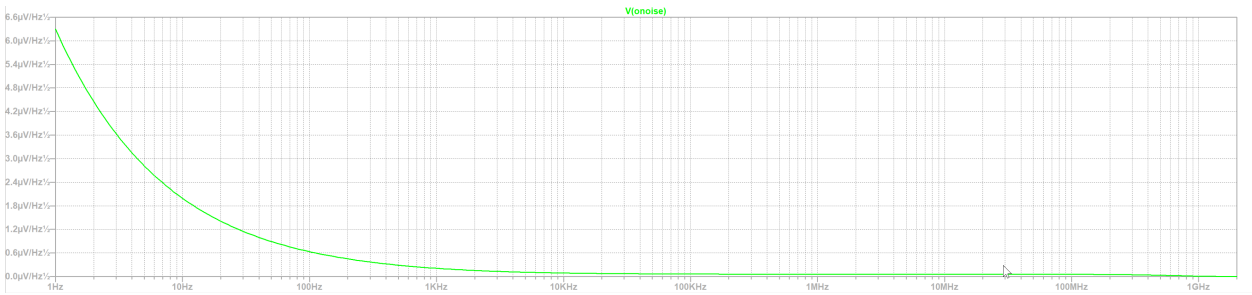


Figure 3.14: Shows the noise simulation result for amplifier chains with LMH6629 and THS3202 in series. $V_{rms} = 1.1mV_{rms}$ at BW 1Hz-0.6GHz

3.3.3 Testing the Amplifier Chain Design Boards

Three amplifier design candidates were simulated. Each of the following boards is used to characterize the amplifier chain design for XRM. The primary difference between the simulated result and the physical measurement comes from the parasitic capacitance and mutual inductance introduced by the board's layout. Parasitic effects affect the overall bandwidth of the design and it is design critical to decrease their effects on the amplifier chains. Both were designed to contain all of the necessary components for each amplifier chain's operation. Most of the designs uses a dual supply. However, for single supply version is tested for comparison of the performance of the LMH6629

amplifier chain design, which requires an additional input bias to be suppled. The bias will be provide by a LT6200 buffer amplifier on board. The extra buffer will change the expected noise VPED was not used.

CHAPTER 4
RESULTS

This section is divided into a several parts. The first discusses noise filtering for the high voltage line on board. The next covers the amplifier test results from the linearity of the amplifier to the noise performance of the amplifier.

4.1 Performance of High Voltage filtering

The High Voltage (HV) filter was characterized to determine the filtering capability and to evaluate the final performance. The instrument used was a network analyzer to measure the S21 parameter for evaluating the Device Under Investigation (DUT).
The experimental results are compared with expected results from the SPICE model, to determine the -3dB point of the filter and the effective roll off.

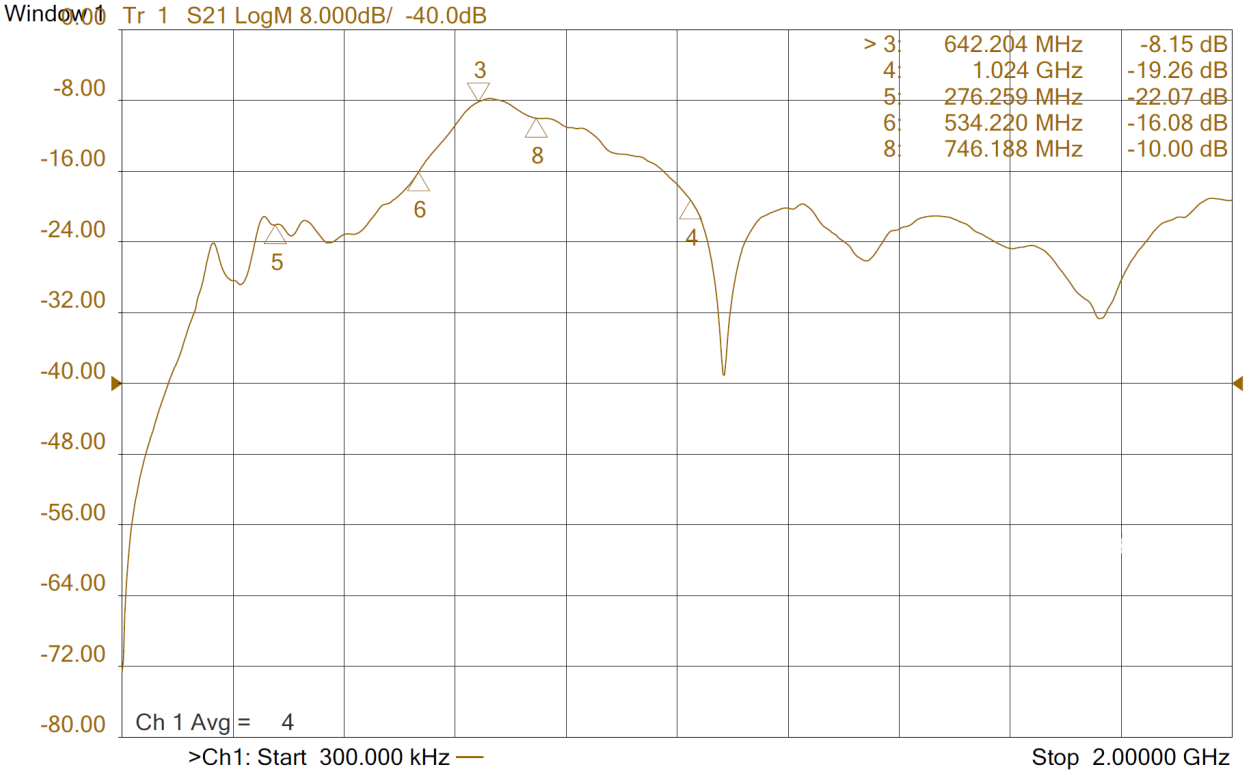


Figure 4.1: Shows the bode plot of high voltage filter used in the final version. The -3dB point was not determined since the network analyzer only goes down to 300KHz and the estimated pole for the filter is at 25KHz.

4.2 Single Channel Version

These tests were performed on a test board to determine the characteristics each of the amplifier chains. These test were performed on two different boards: Little Amplifier Board Rev F and 4ChAmp Board. Each expected gains are specified in each of the result.

4.2.1 Amplifier Chains Gain and Maximum Risetime

This gain measurement was performed on each of the amplifier chains to determine whether the amplifiers were functioning properly. This initial test on the performance included measuring the peak-to-peak voltage to determine the amplifier real gain at low frequency. The test was performed with an arbitrary pulse signal generated using the osciloscope's wavegen signal generator as a source and measurements were done on the same scope. The signal's amplitude can range 10 $\pm$1 mV specified for each experiment. Some outputs have a series resistance to prevent capacitively overloading the output of the amplifier and is typically half of the calculated gain. All expected calculations for each amplifier are shown in the appendix A.1.1-3. For the amplifier maximum rise time, an Avtech 150ps pulse generator is used to generate a 10 $\pm$0.5 mV test pulse to see the transition time.

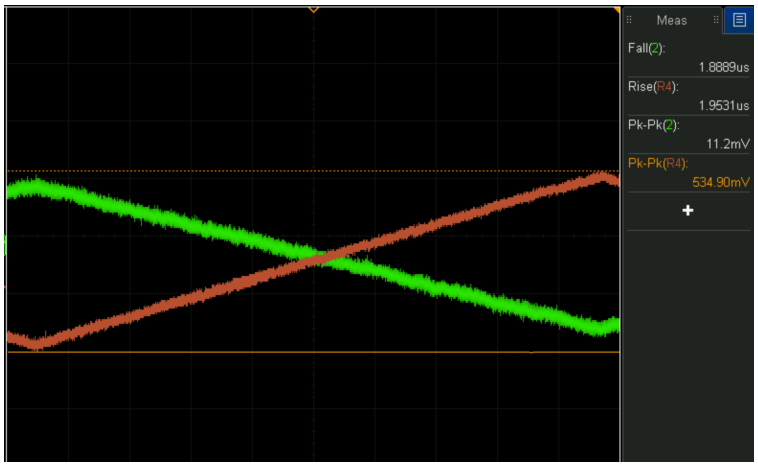


Figure 4.2: Shows the example of a test signal injected during the gain measurement. This result is from the Little Amp Board with two LMH6629 amplifiers in series, injected with a ramping signal of 0V to 10mV.

A compiled table of measured values is shown in Table 4.1

	V_{pp}	Gain	$Gain_{expected}$	Max Risetime ($t_{in_{rise}}$@input:600ps)
LMH/LMH LAB G:110	534.90mV	106.98	109.2	1.2ns
THS/THS 4ChAmp G:25	127mV	25.4	26.2	850ps
LMH/THS LAB G:110	603mV	121.4	110.9	800ps

Table 4.1: The general amplifier measurement done on the amplifier chain. Vpp must be multipled by two due to the series resistance and the load forming a voltage divider.

4.2.2 Amplifier Chain Bandwidth

The bandwidth of the amplifier was determined using an Agilient PNA-L Network Analyzer N5236C . With each test, to be cautious, the input ports were equipped with at least a minimum attenuation of 36dB at the output of each amplifier and a DC block. This was a necessary precaution since all of the amplifiers in testing potentially have DC offset level at the output and the input port can only take a 16V DC voltage. As a consequence, the power level seen on these plots does not reflect the actual gain of the amplifier. The network analyzer was bandwidth calibrated from 300kHz to 2GHz with an attunation of 40dB for all cases to simplify the result.

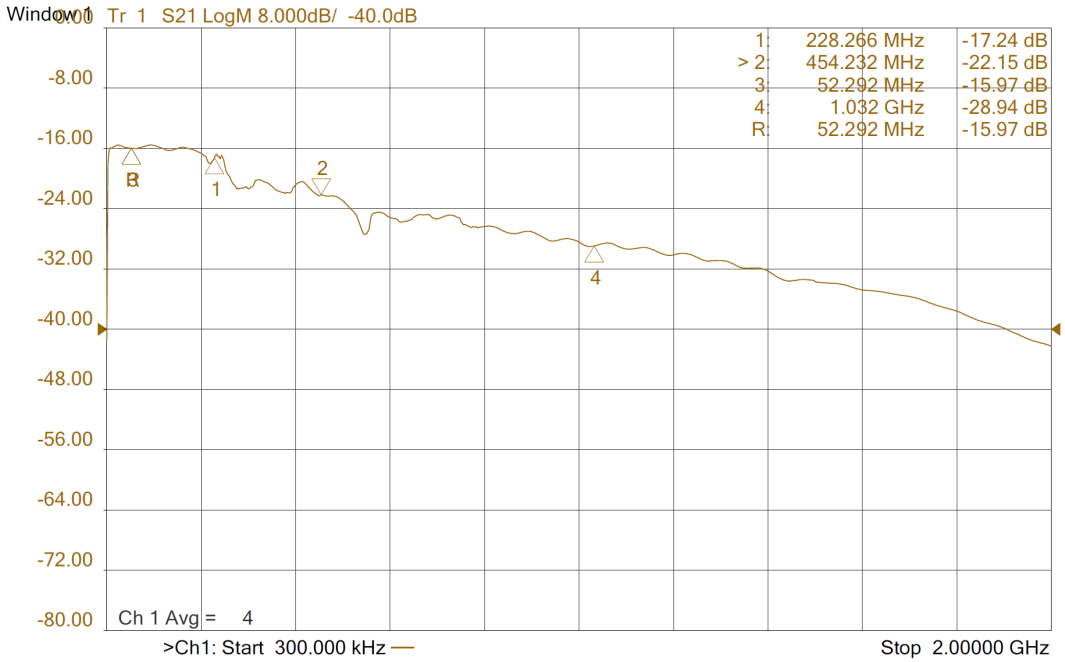


Figure 4.3: Shows the measured S21 parameter of the Little Amp Board with both amplifiers being LMH6629, with non-inverting and inverting configurations. $V_{Supply} = +3.7V, G_{expected}$: 271. The f_{-3dB} was approximately 454MHz.

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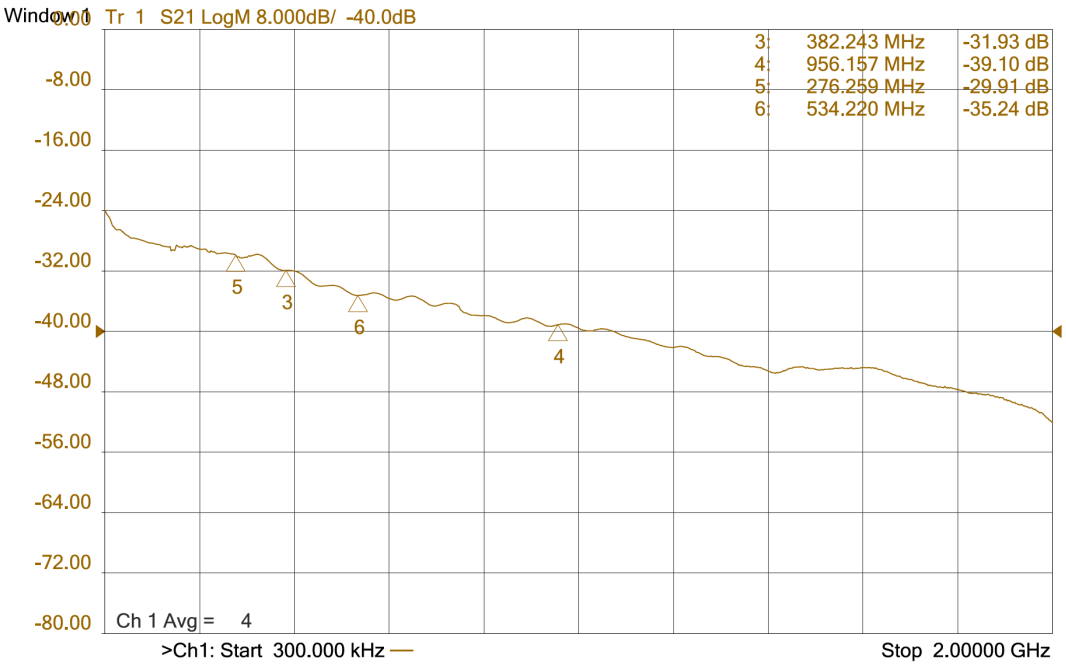

Figure 4.4: Shows the measured S21 parameter of the Little Amp Board with both amplifiers being LMH6629, with non-inverting and inverting configurations. $V_{Supply} = \pm 2.5V, G_{expected} : 110$. The f_{-3dB} was approximately 328MHz.

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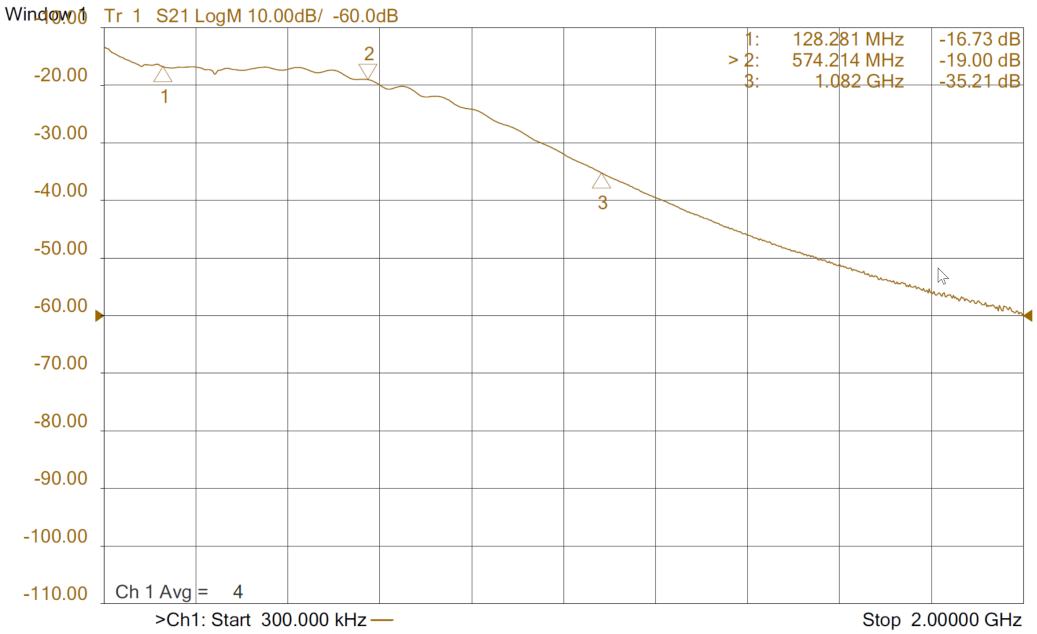

Figure 4.5: Shows the measured S21 parameter of the 4Champ Board with two THS3202 amplifiers. $V_{supply} = \pm 5V, G : 24dB$. The f_{-3dB} was determined to be 574MHz

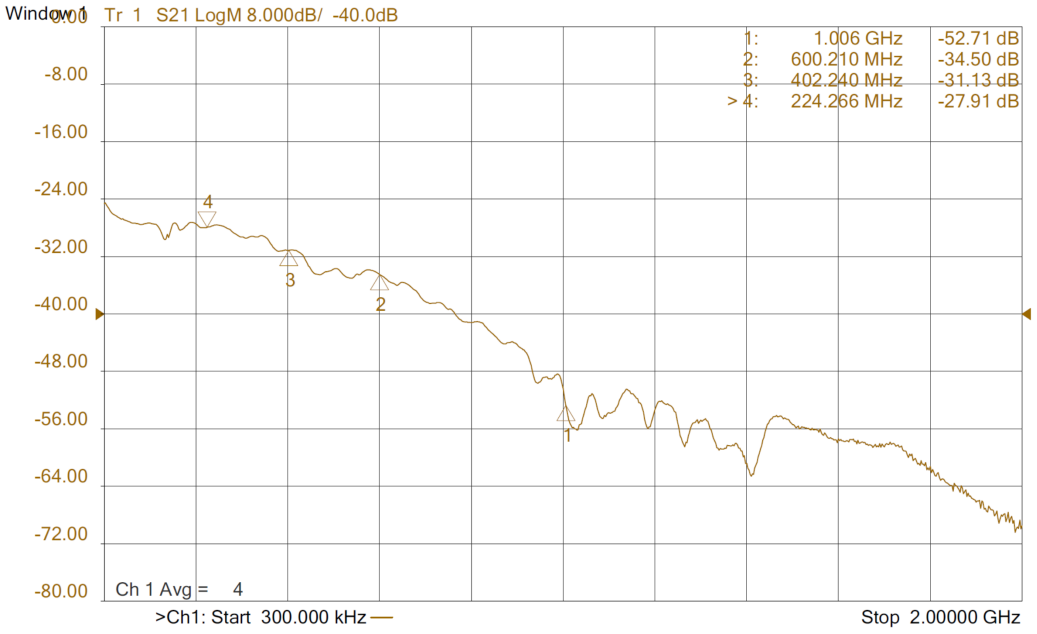

Figure 4.6: Shows the measured S21 parameter of the Little Amp Board with LMH6629 and THS3202 amplifiers, with non-inverting and inverting configurations. $V_{supply} = \pm 3.0V, G : 24dB$. The f_{-3dB} was approximately 402MHz

The bandwidth testing showed that out of all the designs, the 4ChAmp board had the highest f_{-3dB}(574MHz). Any stage amplifier design with an LMH6629 has distortion S21 parameter happening at the higher band that required further investigation. Another source of improvement was to use a separate voltage level for the LMH/THS combination. The THS3201 amplifier has a different overall bandwidth compared to ±3.7V to ±5.0V.

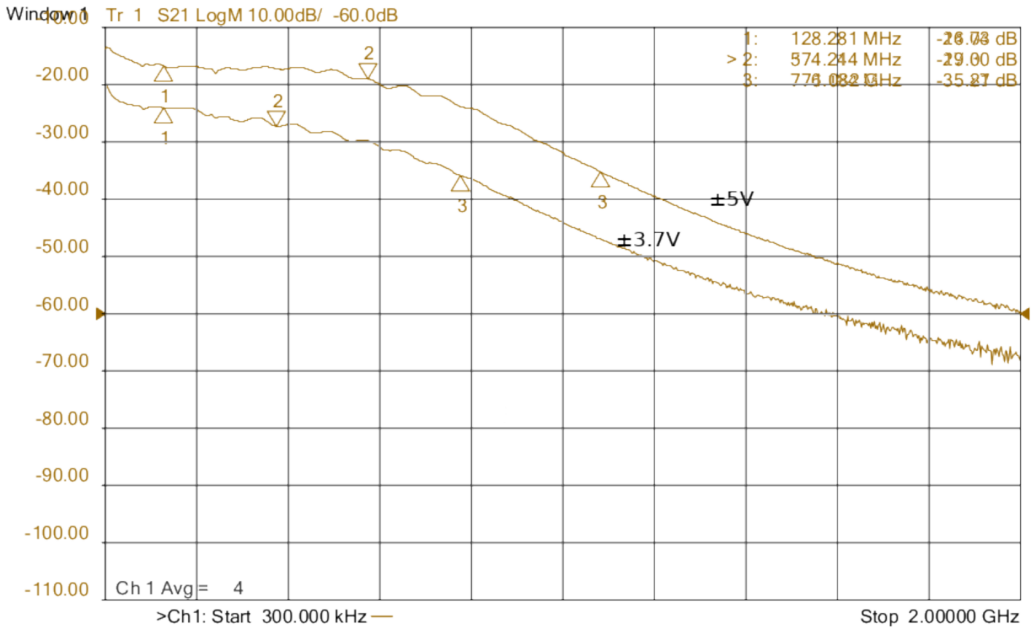

Figure 4.7: The 4ChAmp S21 parameter for $v_{supply} = \pm 3.7V \& \pm 5.0V$. This design used two non-inverting configurations of the THS3202 in a cascaded model. The -3dB point for $\pm 3.7V$ was 374MHz compared to the $\pm 5.0V$, having 574MHz.

This requires a revision to the existing Little Amp Board (LAB) since this design uses a common supply net. This exceeds the absolute maximum dual supply voltage of the LMH6629 amplifier, damaging the amplifier.

4.2.3 Noise Measurement for Amplifier Chains

Voltage noise (V_{RMS}) for each of the amplifier chains was measured using the Infinivision MSOX6004A oscilloscope. The measurements were compared with the simulated SPICE model for verifying the result and estimation of the system's error.

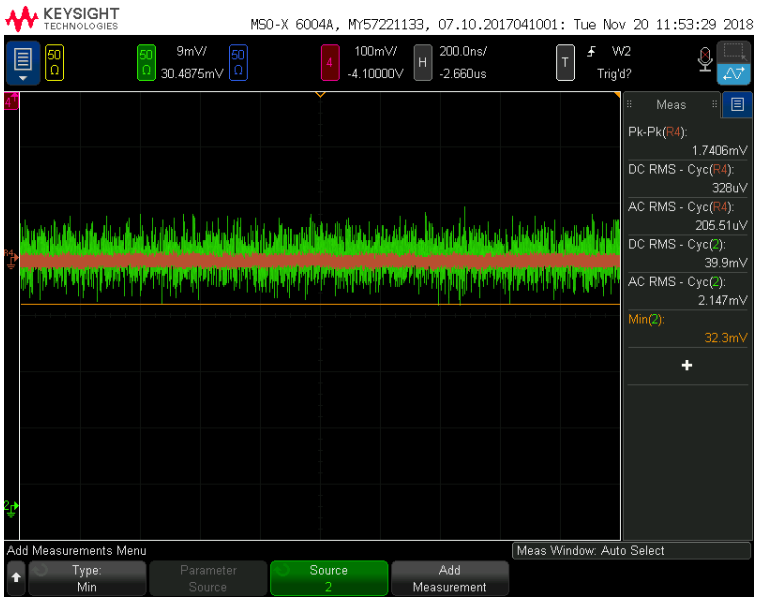

Figure 4.8: Shows the output noise level from the 4ChAmp board with gain of 26.4, with the THS/THS. The DC_{rms} is measured to be $39.9\mu V_{rms}$ and the AC_{rms} is 2.147mV.

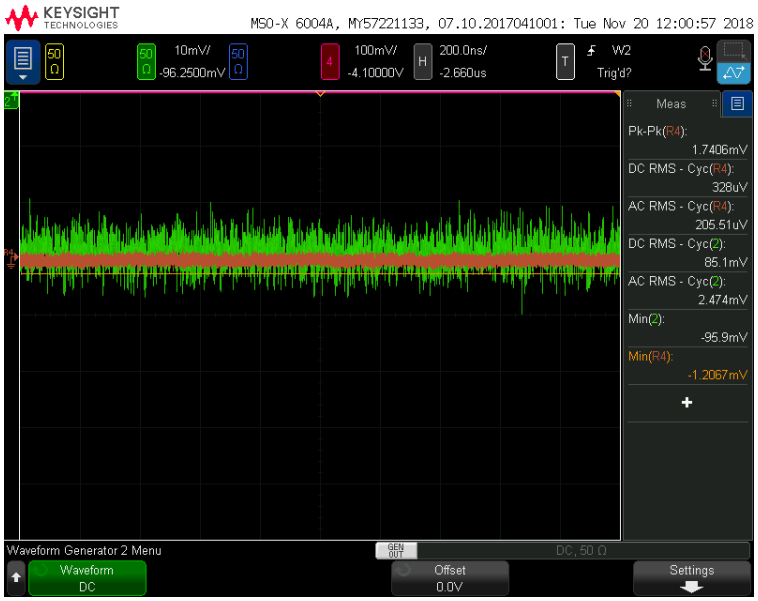

Figure 4.9: Shows the output noise level from the Little Amp board with gain of 110, with the LMH/LMH. The DC_{rms} is measured to be $39.9\mu V_{rms}$ and the AC_{rms} is 2.474mV.

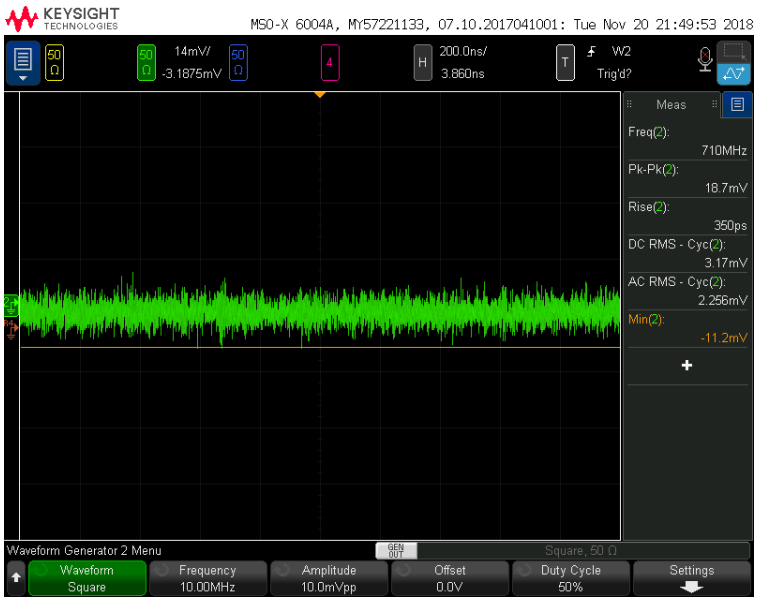

Figure 4.10: Shows the output noise level from the Little Amp Board with gain of 110 with the LMH/THS combination. The DC_{rms} is measured to be $39.9\mu V_{rms}$ and the AC_{rms} is 2.256mV.

To summarize the results, table of the noise measure was generated for each amplifier are shown below.

	DC_{rms}	Inferred Input Noise	Output Noise
LMH/LMH Little Amp Board $\pm 2.5V$ (G:110)	85.1mV	$773\mu V$	$1.12mV_{rms}$
THS/THS 4ChAmp $\pm 5.0V$ (G:26)	39.9mV	$1570\mu V$	$821\mu V_{rms}$
LMH/THS Little Amp Board $\pm 3.0V$ (G:110)	3.17mV	$124\mu V$*	$475\mu V_{rms}$

Table 4.2: The list of the amplifier chain's measured noise at the output. The inferred noise was determined by dividing AC_{rms} by the total gain of the amplifier. The noise calculation was done using the noise analysis given by the SPICE model, the expected AC_{rms} integrated over the bandwidth of the amplifier. For simplicity 600MHz will be the upper bound and 1Hz for the lower bound of the integration. *Requires further investigation

4.2.4 Power Supply Voltage/Current.

Due to the number of amplifiers in a small area, consideration of the amplifier quiescent current draw and supply voltage used is needed to calculate the standby power of the amplifiers. The table below shows the measured values of the amplifier quiescent current for each amplifier chains tested. The load of 50Ω at the output are connected during the data collection and inputs were floated at the time of measurement. All measurements were take from the Keysight E3613a power supply

voltage/current reading that has a read out accuracy of $< 0.1\% + 20$ mV and $< 0.2\% + 4\ mA$ and an output ripple of $< 350\ \mu V_{rms}/2mV_{pp}$

	Voltage (V)	Current (A)	Power (W)
LMH/THS Little Amp Board	±3.0V	0.029/0.029	.360
THS/THS 4ChAmp	±5.0V	0.080/0.080*	.800
LMH/LMH Little Amp Board	3.7V	.055	.203
LMH/LMH Little Amp Board	±2.5V	0.029/0.029	.275

Table 4.3: The measured current/voltage power supply drawn by corresponding amplifier *Note that 4ChAmp uses THS3202 which is a dual amplifier package and so the resulting amplifier current draw should be divided by 2

The LMH/LMH Little Amp Board had the lowest power consumption compared to the other amplifiers tested. The LMH6629 is not rail to rail (Min, Max : $0.87V, V_+ - 0.87V$) as such we cannot DC couple the amplifier with the single supply version. If we were to consider the DC coupled version of the amplifier, the LMH/LMH Little Amp Board Dual supply version was second in terms of quiescent power usage.

4.2.5 SLAC Sensor Output

The signal is generated by an infrared diode and driven by a fast ECL driver for sensor testing. The breakout board can fanout four of the sensor anode's signals that can be fed into the amplifier chain to determine the quality of signal coming from the SLAC sensors. Figure 4.11 shows the resulting scope view of the sensor signal, when a laser pulse is illuminated at the test stand.

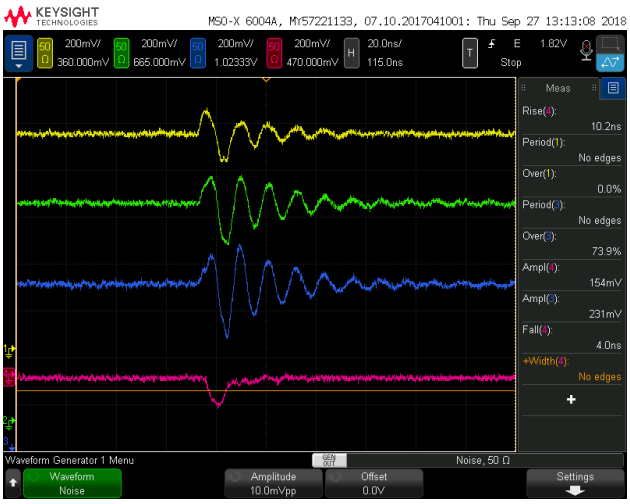

Figure 4.11: The sensor's output amplified. The three top signals are coming from the output of a Little Amp Board (LAB) with G : 271 and the last signal is from a 4champ with G:26.4

CHAPTER 5
CONCLUSIONS

The research evaluated all amplifier designs planned to be used in the next XRM version. The Little Amp and 4ChAmp board were designed with sole purpose of being used in the new amplification stage of the XRM. The simulated result from all of the amplifiers shows potential solutions for XRM amplifier. The PCB boards were developed to test the amplifiers. All of the final designs had issues that do not satisfy final electrical requirements and require additional work to meet them. The amplifier chains for the next iteration of the design should consider faster amplifiers. However, this might require compromises on the current amplifier criteria.

The Little Amp Board requires input to be AC coupled when operating at single supply voltage. From input coupling, the design has a better input reference noise from to the lack of DC flick noise. Out of all of the amplifiers tested, every design with an LMH6629 had input inferred noise better than the THS3202. It is recommended that for the design choice to achieve low noise it should have the LMH6629 as a first stage amplifier. One improvement that can be made is the choice of the Vped buffer (LT6200). The next revision should use a buffer that has a low unity gain bandwidth (-3dB less than 145 MHz). Designing an active low pass filter may be an effective solution.

The 4ChAmp board has a larger input noise reference due to the DC coupled input and the use of a current feedback amplifier on the input stage. The larger current noise at the each input makes it non-ideal for application to the XRM. As such, this amplifier would not be recommended for the first stage. The power consumption by the THS3202 amplifier was double that of the LMH6629 making this board the most power consuming of designs (0.8W) and having the largest input referred noise (1.57mV). The 4ChAmp bandwidth was definitely larger than the other amplifier chains tested (-3dB : 580MHz), however, the total bandwidth could have been better if not for the presences board's stray capacitances. Using the simulation, these stray capacitances were estimated to be on the order of 0.32pF. This is quite difficult to do with the current design capability without undertaking a layout change.

For future reference, there are several items that need to be addressed. Reducing the stray capacitance from the feedback loop in the layout would increase the amplifier design's bandwidth. The simplest solution to this will be using another dielectric material other than the FR-4 ($\epsilon_r = 4.6$). This will significantly increase the cost of production for the board but is the simplest way to solve the issue. Teflon ($\epsilon_r = 2.1$) as a PCB dielectric material is recommended for the next iteration of the sensors fanout board and the amplifier board. The amplifiers require dual rail operation to reduce the overall noise of the system while operating at the ideal DC level. Another recommendation is using an alternative package instead of the SOT23 Package. There are other amplifiers that could potentially give better performance such as the LMH5401 (variable amplifier) or the OPA855 (trans-impedance amplifier), which have better electrical performance for more quiescent current

draw.

However none of these amplifiers were considered during our selection period due the package requirement (16pin PowerPAD(QFN) package, WSON-8 pin). This ultimately means that SOT23 package should be reconsidered for future revisions.

APPENDIX A
AMPLIFIER CHAINS CALCULATION

A.1 Gain Calculation

Note : All resistors had tolerance value is 1%

A.1.1 4ChAmp Board (THS3202x2) Gain Calculation

$$A = g1g2$$

$$A = \left(1 + \frac{R_{f1}}{R_{g1}}\right)\left(1 + \frac{R_{f2}}{R_{g2}}\right)$$

$$A = \left(\frac{(1 + \frac{412\Omega}{59\Omega})}{(1 + \frac{412\Omega}{120\times10^3})}\right)\left(\frac{(1 + \frac{412\Omega}{270\Omega})}{(1 + \frac{412\Omega}{120\times10^3})}\right) = 26.4$$

A.1.2 Little Amp Board (LMH6629x2) Gain Calculation

$$A = g1g2$$

$$A = \left(1 + \frac{R_{f1}}{R_{g1}}\right)\left(\frac{R_{f2}}{R_{g2}}\right)$$

$$A = \left(1 + \frac{450\Omega}{49.9\Omega}\right)\left(\frac{499\Omega}{49.9\Omega}\right) = -110.1$$

A.1.3 Little Amp Board (LMH6629/THS3201) Gain Calculation

$$A = g1g2$$

$$A = \left(1 + \frac{R_{f1}}{R_{g1}}\right)\left(\frac{R_{f2}}{R_{g2}}\right)$$

$$A = \left(1 + \frac{450\Omega}{49.9\Omega}\right)\left(\frac{499\Omega}{49.9\Omega}\right) = -110.1$$

A.2 Example Noise Calculation

A.2.1 4ChAmp Board - THS3202x2 V_{rms} Calculation (Gain :26.4)

$$En_{1st} = \sqrt{\left(2\frac{nV}{\sqrt{(Hz)}}\right)^2 + \left(1.65\frac{nV}{\sqrt{(Hz)}}\right)^2 + 4(1.381\times10^{-23}J/K)(293.15K)(412\Omega) + 4(1.381\times10^{-23}J/K)(293.15K)(59\Omega)}$$

$$= 22.5897nV/\sqrt{Hz}$$

$$En_{2nd} = \sqrt{\left(\left(22.5897\right)^2 + \left(2\right)^2 + \left(1.65\right)^2 + 4(1.381 \times 10^{-23} J/K)(293.15K)(49.9\Omega) + 4(1.381 \times 10^{-23} J/K)(293.15K)(\frac{(450\Omega)(49.9\Omega)}{450\Omega + 49.9\Omega})\right)}$$

$$= 152nV/\sqrt{Hz}$$

APPENDIX B
SENSORS CALCULATION

B.0.1 Detector's Capacitance Estimate

Bias Voltage = -60V,
Estimated value of resistivity of the silicon substrate: $\rho = 5k\Omega \times cm$
and the mobility of majority charge carrier (electron, assumed crystaline medium)($\mu = 1400cm^2/(Vs)$)
$A = 6700 * 2415\mu m^2$

$$C_d = \sqrt{\frac{\epsilon_0 \epsilon_{si}}{2\pi\rho\mu|V|}} A$$

$$C_d = 4.7pF$$

APPENDIX C
LOW/HIGH DENSITY PINOUT

C.1 Low Density Pinout

low-density case (80 pins)			
pin			pin
1	GND	POWER	2
3	2.7 or 1.7	3.0 or 0.0	4
5	POWER	GND	6
7			8
9	GND	POWER	10
11	2.6 or 1.6	3.1 or 0.1	12
13	POWER	GND	14
15			16
17	GND	POWER	18
19	other	other	20
21	POWER	GND	22
23			24
25	GND	POWER	26
27	2.5 or 1.5	3.2 or 0.2	28
29	POWER	GND	30
31			32
33	GND	POWER	34
35	2.4 or 1.4	3.3 or 0.3	36
37	POWER	GND	38
39	other	other	40
41	other	other	42
43	GND	POWER	44
45	2.3 or 1.3	3.4 or 0.4	46
47	POWER	GND	48
49			50
51	GND	POWER	52
53	2.2 or 1.2	3.5 or 0.5	54
55	POWER	GND	56
57			58
59	GND	POWER	60
61	other	other	62
63	POWER	GND	64
65			66
67	GND	POWER	68
69	2.1 or 1.1	3.6 or 0.6	70
71	POWER	GND	72
73			74
75	GND	POWER	76
77	2.0 or 1.0	3.7 or 0.7	78
79	POWER	GND	80

Figure C.1: Shows the low density connection. It was intentionally designed to be symmetrical so the board could be connected on top or bottom.

C.2 High Density Pinout

high-density case (80 pins)			
pin			pin
1	GND	POWER	2
3	2.7	3.0	4
5	POWER	GND	6
7	1.7	0.0	8
9	GND	POWER	10
11	2.6	3.1	12
13	POWER	GND	14
15	1.6	0.1	16
17	GND	POWER	18
19	other	HV	20
21	POWER	GND	22
23	2.5	3.2	24
25	GND	POWER	26
27	1.5	0.2	28
29	POWER	GND	30
31	2.4	3.3	32
33	GND	POWER	34
35	1.4	0.3	36
37	POWER	GND	38
39	other	other	40
41	other	other	42
43	GND	POWER	44
45	2.3	3.4	46
47	POWER	GND	48
49	1.3	0.4	50
51	GND	POWER	52
53	2.2	3.5	54
55	POWER	GND	56
57	1.2	0.5	58
59	GND	POWER	60
61	other	other	62
63	POWER	GND	64
65	2.1	3.6	66
67	GND	POWER	68
69	1.1	0.6	70
71	POWER	GND	72
73	2.0	3.7	74
75	GND	POWER	76
77	1.0	0.7	78
79	POWER	GND	80

Figure C.2: Shows the high density connection. It was intentionally design to be symmetrical so the board could be connected on top or bottom.

APPENDIX D
SCHEMATIC AND LAYOUT

D.1 Little Amp Board Rev F

Schematic links : https://www.phys.hawaii.edu/~mza/PCB/misc/little-amp-board.revF.schematic.pdf
Layout Link https://www.phys.hawaii.edu/~mza/PCB/misc/little-amp-board.revF.layout.pdf
Gerber Link : https://www.phys.hawaii.edu/~mza/PCB/misc/little-amp-board.revF.fab-gerbers.zip

D.2 2ChAmp Board

Schematic links :
Layout Links :
Gerber Link : https://oshpark.com/shared_projects/5H4pWcc4.

D.3 4ChAmp Board

Schematic links :
Layout Links :
Gerber Link : https://oshpark.com/shared_projects/QGHyecPx

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